先進封裝與晶圓級封裝的基本原理
CSP, WLP, Flip Chip, MCP/SiP & Lead Free

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CSP (Chip Scale Package / Chip Size Package)

前言

- 由於晶片設計越趨複雜與微小化，封裝方式與技術也同步跟著進入世代交替，過去採用塑膠平面晶粒承載封裝（QFP）的數位相機用控制晶片、CompactFlash、無線網路產品等，均過度到球狀閘陣列（BGA）封裝；而過去採用BGA封裝的中央處理器（CPU）、繪圖卡與晶片組等，亦進階到覆晶封裝；至於手機用相關零組件、DDRII均將大規模採用晶圓級封裝（Chip Scale Package；CSP），因此，預計到2007年的4年內，BGA與CSP等高階封裝應用，將獨領風騷，依Electronic Trend Publications的統計資料顯示，BGA與CSP兩者，在2002 2007年間，產值的年平均複合成長率，將分別高達13.39%與17.58%。
- 歷經近年來年來的半導體產業不景氣的考驗後，國際IDM大廠獲利困難，紛紛傾向於逐步釋出非核心的後段封測業務，僅保留前段的IC設計與製造，使封測業務外包趨勢，近年來日益明顯。加上因BGA與CSP等高階封裝所需投入的成本日益增加，因此諸多IDM大廠在無力負荷的情況下，預期釋出高階後段訂單比重，將日益提高。年平均複合成長率部份，BGA為18.77%，至於CSP更高達20.45%，因此就整體IDM大廠所釋出的委代封測訂單中，BGA與CSP等高階封裝將成為其中最大宗。

資料來源： Digitimes,

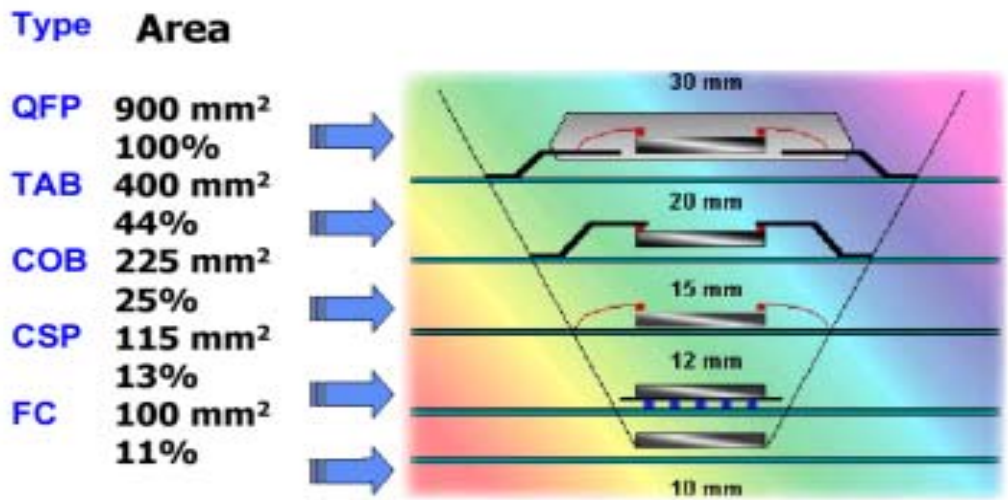
CSP Demands

- 依Electronic Trend Publications調查顯示，2006年全球CSP的市場需求量將達126.71億顆，較2002年的45.85億顆，成長276%。由於手機等網路通訊相關產品愈來愈標榜小型封裝型態，此外DDRII的興起，頻率多在400MHz以上，腳數多在100腳以下，使CSP封裝型態的市場需求量有明顯增加的跡象。 Electronic Trend Publications估計， 2004年為88.71億顆，2005年一舉突破百億顆關卡，達103.73億顆，2006年更可望增加到126.71億顆。
- CSP封裝一般的定義廣泛，因此此種封裝體的外型，可以是類似QFN（Quad Flat No-Lead）的金屬引腳，也可以是像BGA（Ball Grid Array；閘球陣列封裝）的錫球。而CSP封裝的應用領域，包含通訊晶片、繪圖晶片、微控制器（MCU）、數位訊號處理器（DSP）、記憶體，以及邏輯與類比等多種IC，並以手機零組件的封裝為多。
- 但若以封裝的型式加以區分，其一則為Substrate CSP，以基板(rigid or Flex)為支撐，呈現陣列型式（Array-style），類似小型BGA。第二為Leadframe CSP，顧名思義，是以導線架為支撐基材，也由於這種封裝的製程困難度較低，加上所需更換的材料較少，因此適用於射頻（RF）晶片的封裝。第三則為Wafer Level CSP，即晶圓級的CSP，有助於進一步縮減封裝體積。

資料來源： Digitimes,

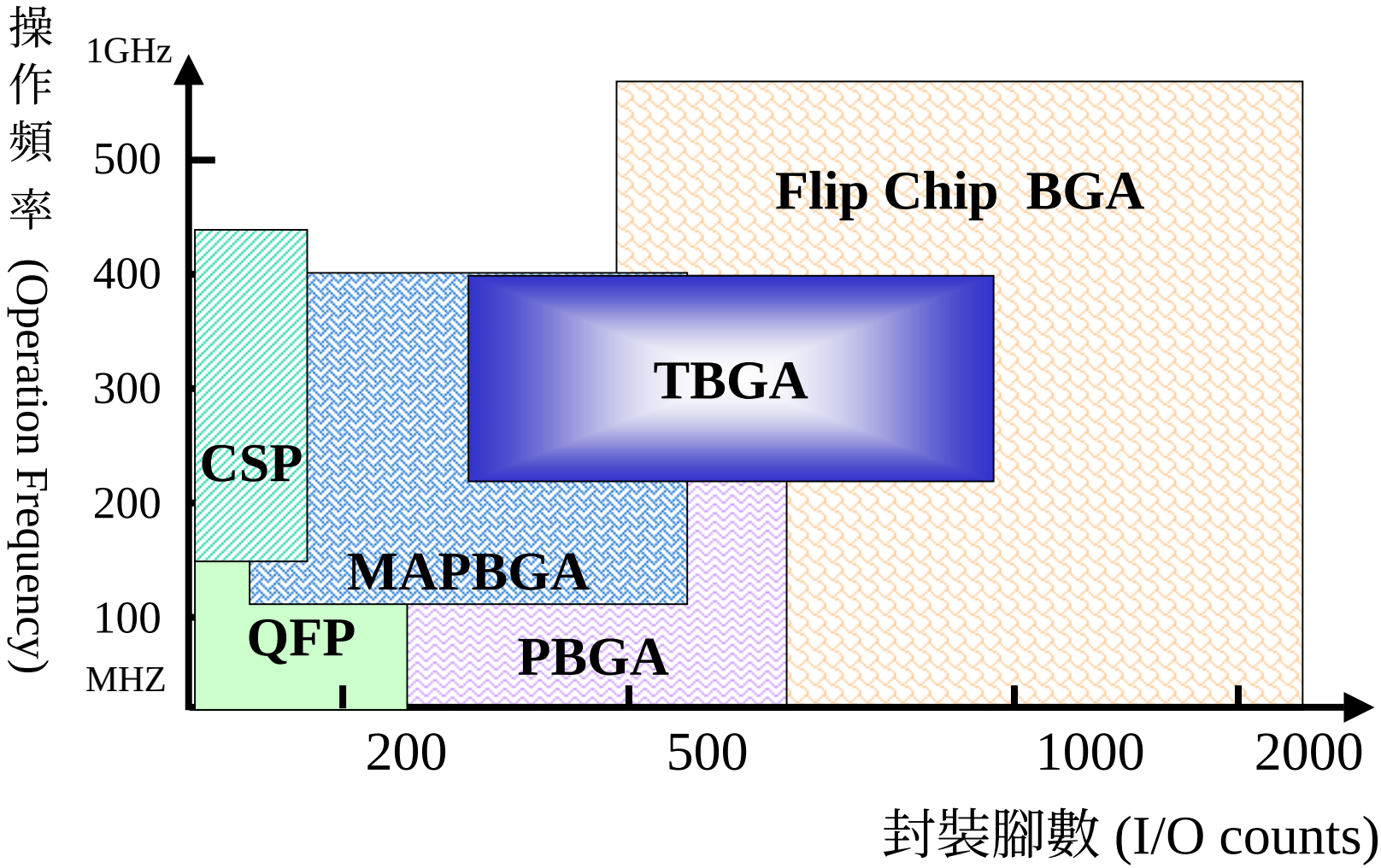
Definition & CSP

- EIA (Electronic Industries Association) and IPC (Interconnecting and Packaging electronic Circuit) in J-Std-012 “Implementation of Flip Chip and CSP Technology”: ...封裝後不超過原始晶片尺寸面積的1.2倍並可直接利用表面貼著技術加工者(direct surface mountable)
- 1993年才引用於產業中



Frequency, I/O counts vs. Packaging Technology

頻率、腳數 vs. 封裝技術



IC Package for mobile phone and Portable devices

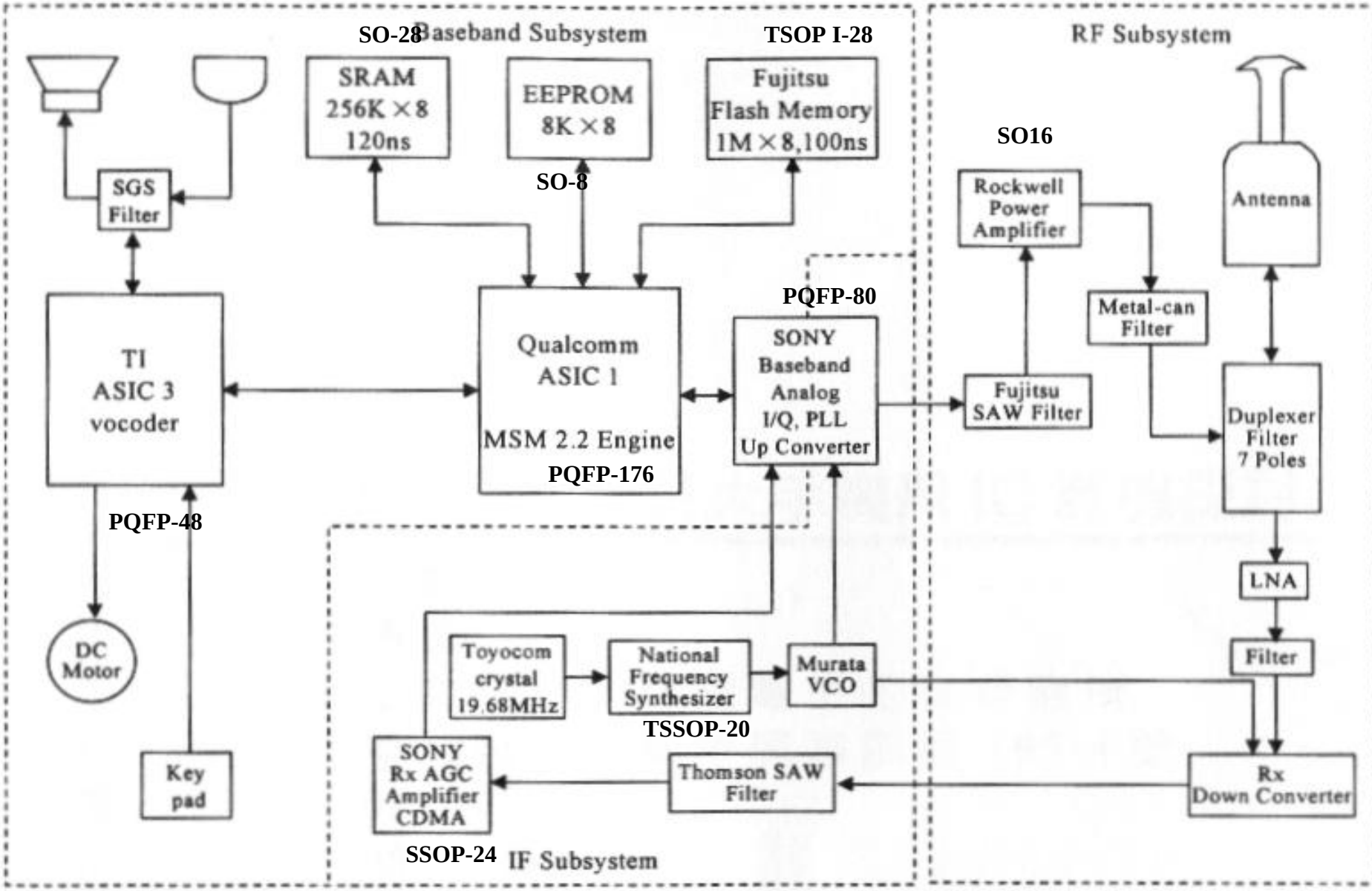
Section	pin count	applications	Packages	Driving force
RF	8 - 48	Power Amplifier	SON, QFN	smaller
				lower cost
		LNA, Mixer	TE-TQFP	smaller footprint
		Xceiver	MAPBGA	
			QFN	
		Modules	Laminate	solder joint reliability
			Flip chip	
IF	20 - 100	Synthesizer,	MAPBGA	smaller
		Modulator	TFBGA	
		Analog	QFN	
Digital	8 - 48	Memory	TFBGA	smaller
		(Flash, ROM, RAM)	MAPBGA	
			Stacked chip	
	32 - 200	ASIC,	MAPBGA	
		Power Management	TFBGA	
		CODEC	COF-BGA	
		Baseband processor	MCM-BGA	

Mobile Phone IC Function Description

項 目	功 能 說 明	
傳送器 接收器	發射訊號、接手訊號。	
功率放大器	藉由放大功率、產生高頻訊號。	Rth, electrical performance
合成器	用以產生固定頻率信號。	
A/D、D/A、 調變解調器	射頻降為中頻、類比訊號轉為數位訊號；或是數位訊號轉為類比訊號、中頻轉為射頻。	
數位訊號 處理器	語音訊號壓縮 / 解壓縮、錯誤更正編 / 解碼、資料加密 / 解密、解調變、頻道等化、資料格式封裝。	
微控制器	人機介面控制、通訊協定管理。	
記憶體	包括快閃記憶體、靜態隨存記憶體的功能。	

Source: Dataquest

Samsung SCH-300 Phone Block Diagram



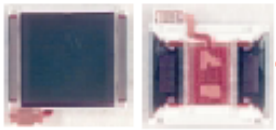
ANATOMY OF A SYSTEM - MOBILE PHONE

LEGEND

Category $ and % Breakdown
- Examples
- Players
- Region
- Drivers

Input/Output Devices | $4 | 3%

- LCD, OLED, Microdisplays
- Casio, Sharp, Three-Five Systems
- Mostly Japan, Korea, Taiwan
- Color and Higher Resolution



Mechanical Components | $6 | 4%

- ABS/PC, Metal
- Chomerics
- Many Local Suppliers
- Weight and Assembly Cost

Power Devices | $7 | 5%

- Li-Ion, NiMH, NiCd Batteries
- Sony, Matsushita, Sanyo
- Japan
- Greater Power Density

Microwave Components | $14 | 9%

- VCO, Filter, Crystal
- Murata, Matsushita, CTS
- Worldwide, but Japan strong
- Smaller Size, RF Modules

Active Components | $48 | 32%

- DSP, Memory, Transceiver
- TI, Samsung, Philips
- America (DSP), Asia (SRAM), Europe (RF)
- Silicon and RF Integration

Passive Components | $6 | 4%

- Capacitors, Resistors, Connectors
- AVX, TDK, Tyco
- Worldwide Production
- Integrated Passives and 0201

Substrate | $3 | 2%

- Microvia, FR-4, Flex
- Matsushita, Compeq, AT&S
- Japan, Asia and Europe
- Increasing Attachment Pad Density

Assembly | $10 | 7%

- Board and Box Assembly
- Flextronics, Celestica
- Worldwide
- Move to Contract Assembly

Value Add | $54 | 35%

- R&D, SGA, EBIT
- Nokia, Motorola, Ericsson
- Worldwide
- Virtual OEM's

資料來源： Prismark, 2002

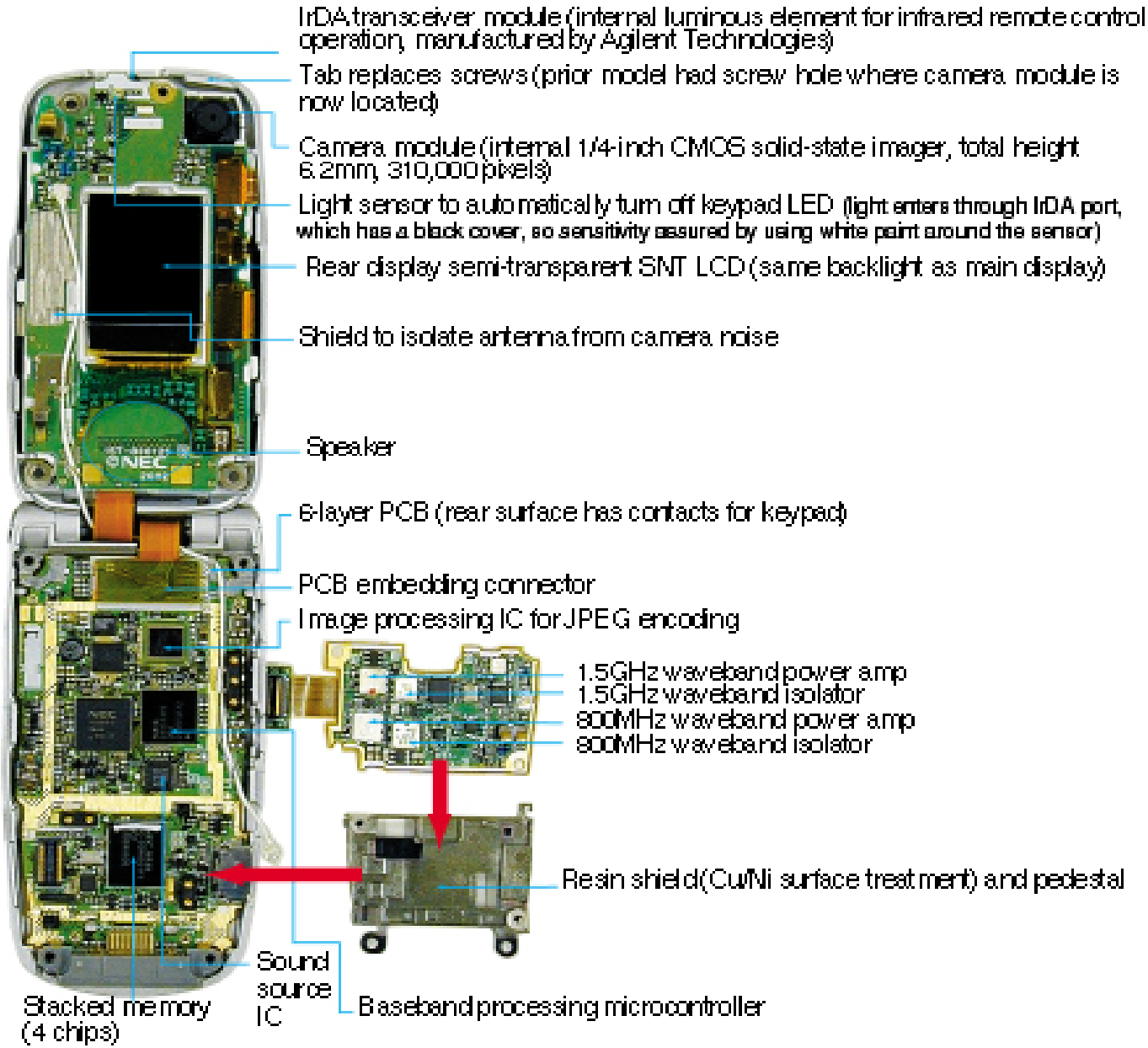


Fig 3 Inside the Mova N504iS The small PCB to the lower right is mounted on the pedestal below it, inside the bottom case (keypad case).

手機市場中的半導體大趨勢

- 近十年來，電子產業以及半導體產業中最激動人心智的大事，莫過於手機的發展。手機的發展有幾個獨特的地方：首先，它的每年運量已達每年5億支的數字，即使預計將來單位運量的年度複合成長率只能維持在7　8%，但是與次高運量的PC相較，仍然有3　4倍之多，因此絕對是兵家必爭之地。
- 再者，手機由於是移動運用，所以在電源管理及尺寸(form factor)上是錙銖必較；而且，手機雖然是屬於通訊類，但是消費性電子產品的個性鮮明，所以成本的要求也是極端嚴苛。這些需求都驅策著其上游產業半導體往其極限能力發展。
- 其三，手機產業由於目前還沒有定於一尊的供應商，像是英特爾或是微軟之於PC，沒有壟斷的規格，容許百花齊放、百鳥爭鳴的系統解決方案.，所以到目前於系統規格、零件規格等方面等，都有為數眾多的廠家參與競爭。這個局面，短期間還不會了結。
- 龐大的利益、嚴苛的要求以及開放的競爭平台，這3個環境條件使得手機系統及其半導體元件的發展進入大鳴大放的時期。
- 有幾個有趣的趨勢關係著半導體與手機廠商的交互作用:

資料來源： Digitimes

半導體與手機廠商趨勢關係

1. 首先是零件的整合:簡化成單一套片,不同的晶片材料（Si，GaAs,..),無法在晶圓生產過程整合的以MCP的方式整合。目前照相手機的鏡頭模組，至少含有CMOS Sensor、鏡頭等基本單位，另外的影像處理控制器是否要包含於其中，或先與其所需支援的記憶體形成一小影像處理模組，再併入較大之鏡頭模組等，都有廠商提供不同的方案。相同的狀況也發生例如Java 3D遊戲等模組。
2. 第二個趨勢是特色應用（feature application）成為手機市場競爭主軸。電子系統的傳統性能競爭指標是速度，在手機應用，這當然是容許許多特色應用的基本平台，但是卻不是手機市場激烈競爭的主軸。

Four Groups in CSPs

1. *Customized-lead-frame-based CSP*

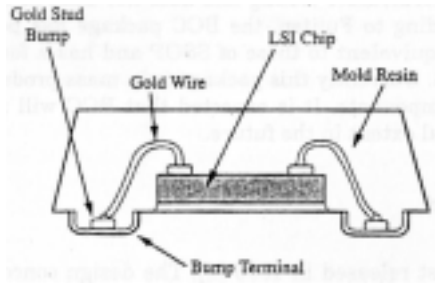
2. *CSP with flexible substrate*

3. *CSP with rigid substrate*

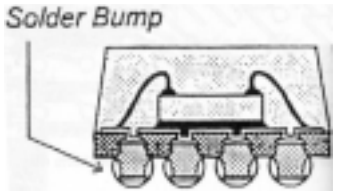
4. *Wafer-level redistribution CSP*

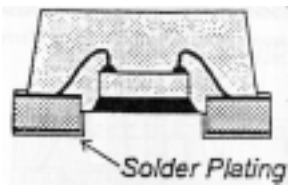
Customized-lead-frame-based CSP

- Fujitsu's Small Outline No-Lead/C-Lead Package(SON/SOC)
- Fujitsu's Bump Chip Carrier(BCC)



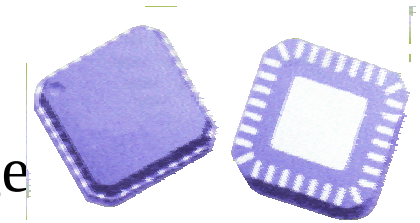
- Fujitsu's MicroBGA and Quad Flat Nonlead(QFN) Package





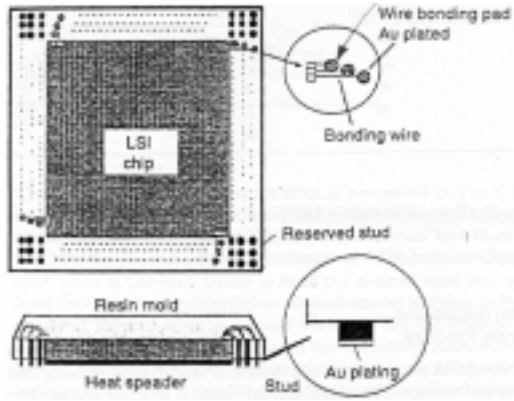
- Hitachi Cable's Lead-on-Chip Chip Scale Package(LOC-CSP)

- Anam/Amkor MicroLeadframe Package



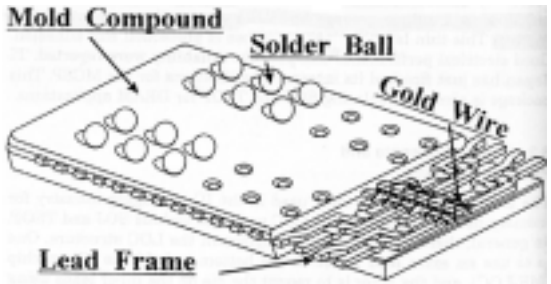
Customized-lead-frame-based CSP

•Hitachi Cable's Micro Stud Array(MSA)



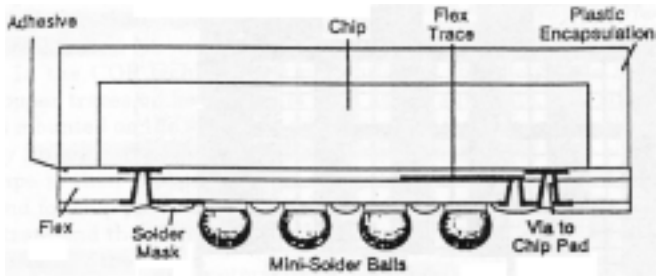
•LG Semicon's Bottom-Leaded Plastic Package(BLP)

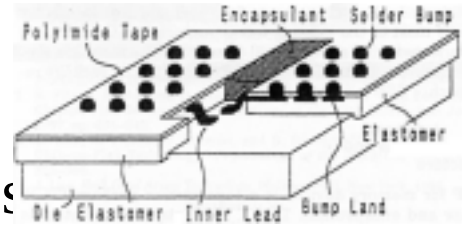
•TI Japan's Memory Chip Scale Package with LOC(MCSP)



CSP with flexible substrate

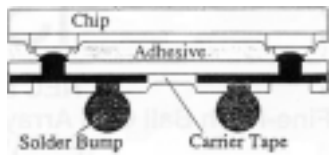
- 3M's Enhanced Flex CSP
- General Electric's Chip-On-Flex Chip Scale Package(COF-CSP)



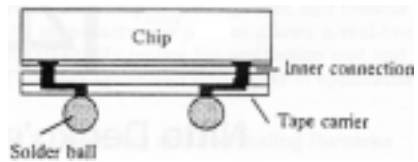


- Hitachi's Chip Scale Package for Memory Devices

- IZM's *flex*PAC
- NEC's Fine-Pitch Ball Grid Array(FPBGA)

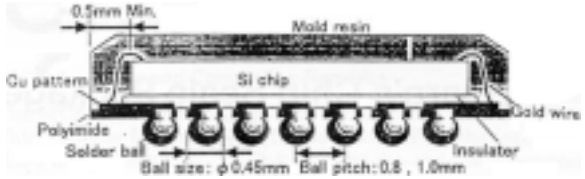


- Nitto Denko's Molded Chip Size Package(MCSP)



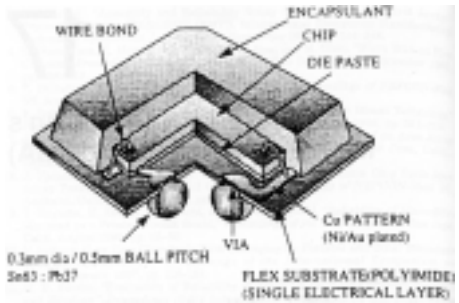
CSP with flexible substrate

- Sharp's Chip Scale Package

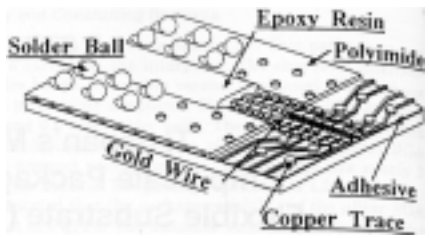


- Tessera's Micro-Ball Grid Array(μBGA)

- TI Japan's Micro-Star BGA(μStar BGA)



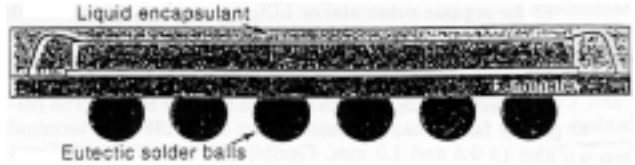
- TI Japan's Memory Chip Scale Package with Flexible Substrate(MCSP)



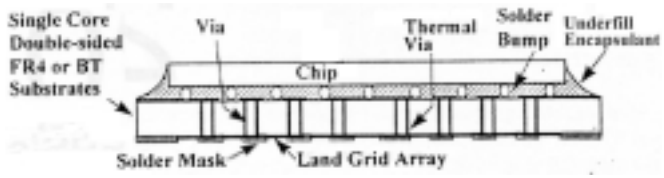
CSP with rigid substrate

- Amkor/Anam's ChipArray Package

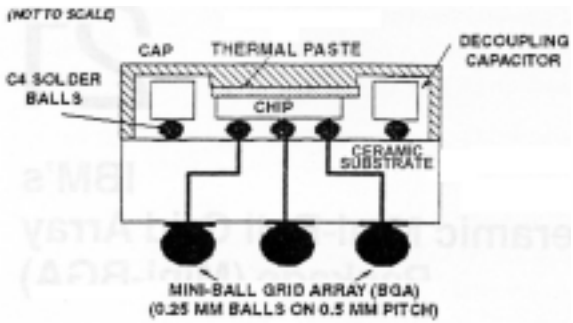
  LFBGA, miniBGA

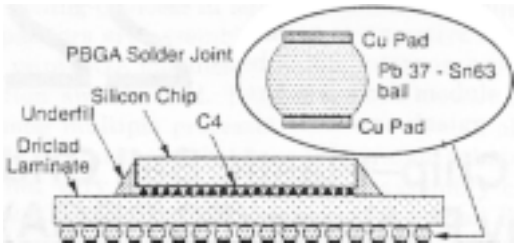


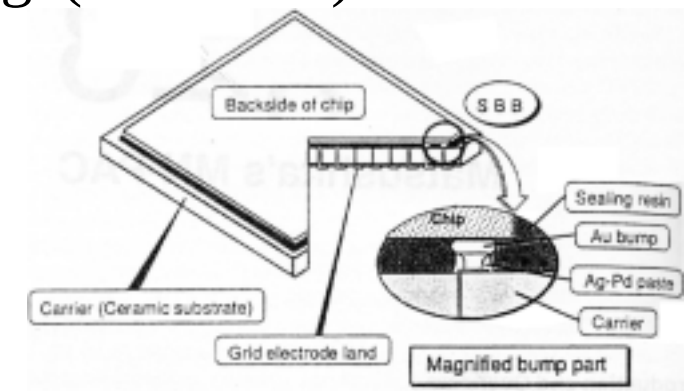
- EPS's Low-Cost Solder-Bumped NuCSP



- IBM's Ceramic Mini-Ball Grid Array Package(Mini-BGA)
- IBM's Flip Chip-Plastic Ball Grid Array Package(FC-PBGA)
- Mitsushita's Stud Bump Bonding Package(MN-PAC)

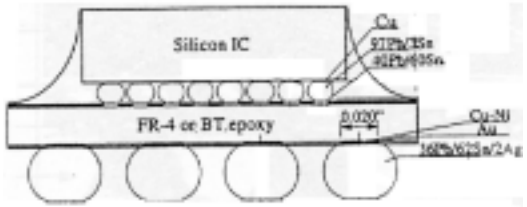


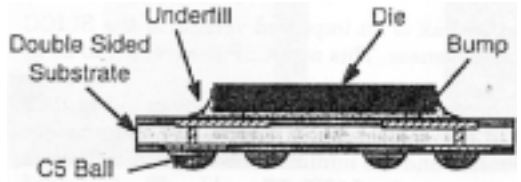


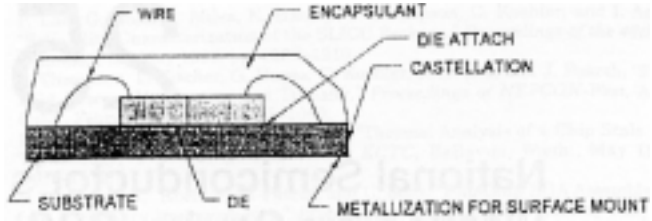


CSP with rigid substrate

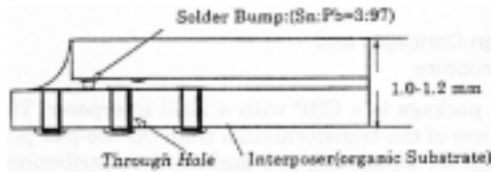
- Motorola's SLICC and JACS-Pak



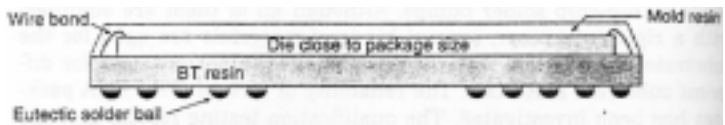


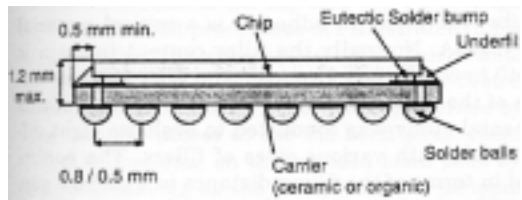


- National Semiconductor's Plastic Chip Carrier(PCC)
- NEC's Three-Dimensional Memory Module(3DM) and CSP
- Sony's Transformed Grid Array Package(TGA)
  (one kind of LGA:Land Grid Array)



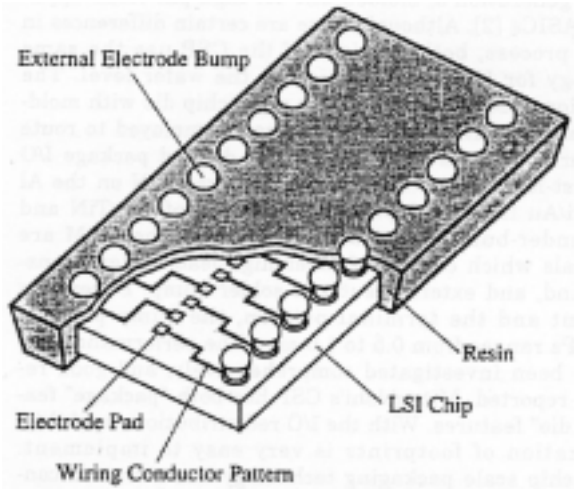
- Toshiba's Ceramic/Plastic Fine-Pitch Ball Grid Array Package(C/P-FBGA)





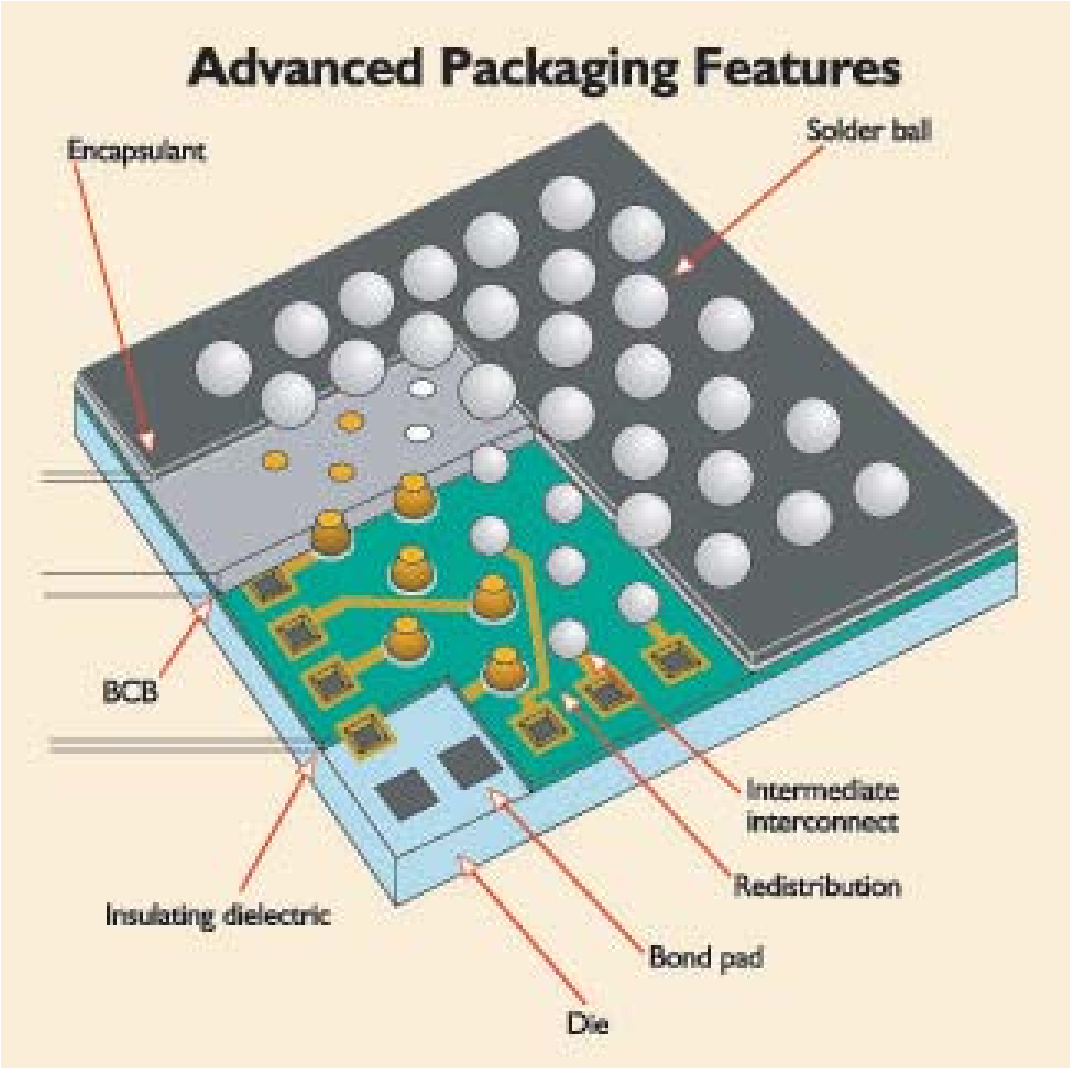
Wafer-level redistribution CSP

- ChipScale's Micro SMT Package(MSMT)
- EPIC's Chip Scale Package
- Flip Chip Technologies's *Ultra*CSP
- Fujitsu's *Super*CSP(SCSP)
- Mitsubishi's Chip Scale Package



- National Semiconductor's MSMD
- Sandia National Laboratories's Mini Ball Grid Array(μBGA)
- ShellCase's Shell-PACK/Shell-BGA

Wafer Level Package (WPL)
Wafer Level Chip Scale Package



Wafer Level CSP

- The term "wafer-level packaging" (WLP) entered the microelectronics industry's lexicon in the late 1990s.
- WLP is an advanced packaging technology in which the die interconnects are manufactured and tested on the wafer, then singulated by dicing for assembly in a surface mount line.
- Devices that are packaged at the wafer level are more generally termed **wafer-level chip size packages (WLCSP)**.
- For small die, the thermal mismatch between the silicon and its circuit board substrate is less problematic because of the small distances involved.
- A chief limitation to the pin count for bumped WLPs has been less than about 60 balls because of limited solder ball fatigue lifetimes.

ITRS forecast of minimum pitches of various mounting technologies for leading edge ICs

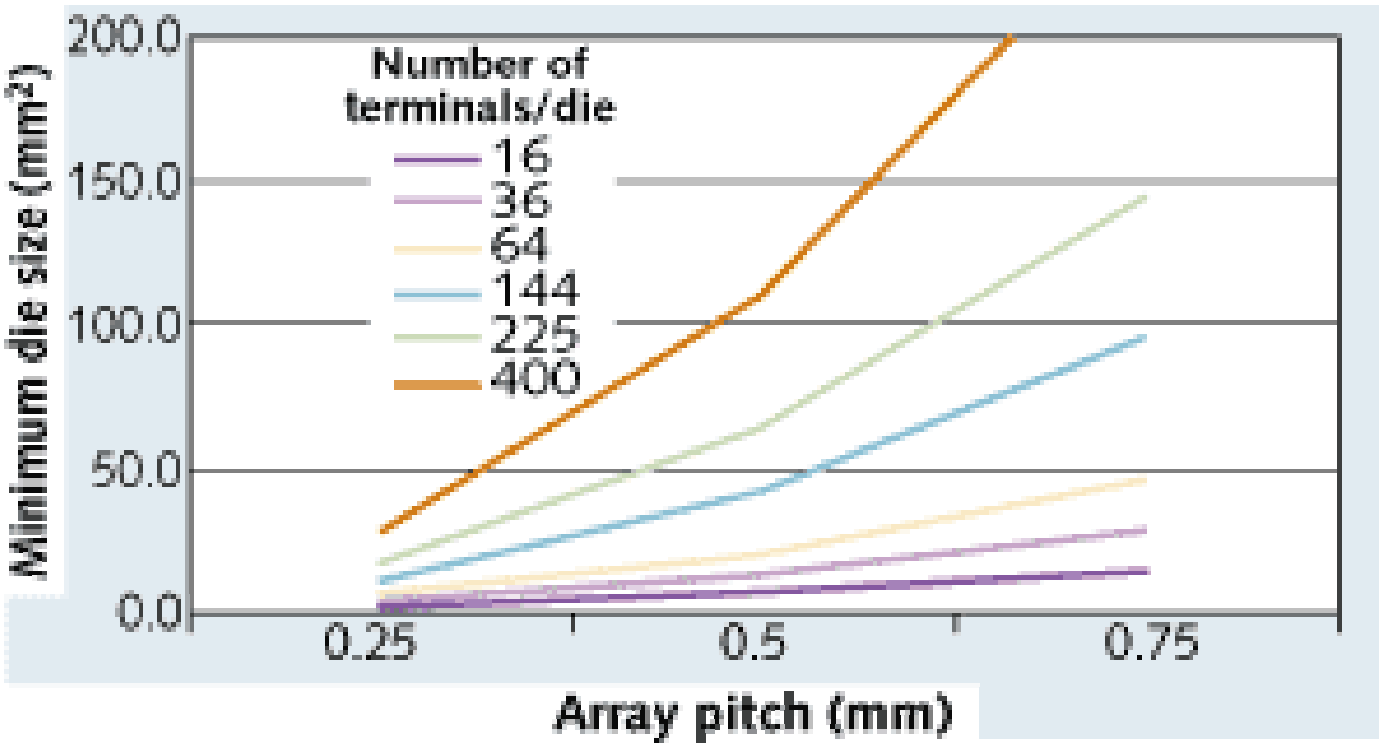
- flip chip is applied to those die with area pad pitch of less than 250 µm and ball diameters less than 120 µm. JEDEC has defined a "die size chip scale package" that describes the WLP phenomenon.

Chip interconnect pitch (µm)							
	2001	2002	2003	2004	2005	2006	2007
Wirebond: ball	45	35	30	25	20	20	20
Wirebond: wedge	40	35	30	25	20	20	20
Flip chip (area array)	160	160	150	150	130	130	120
Flip chip (peripheral)	150	130	120	110	100	90	80
WLP	500	400	400	400	300	300	300

Wafer Level Burn-in and Test

- A cost-effective test strategy is based on fab process maturity, device type complexity, yield management effectiveness and an appreciation of the application domain requirements.
- Test strategies range from no test at all to full testing of all AC and DC parameters, as well as functional and structural testing.
- Testing done at the wafer level traditionally has been a minimal test to simply ascertain gross failure.
- The entire final test suite should be performed at the wafer level to realize cost efficiencies.

Plot of minimum die size for various I/O per die at several pitches

- 

晶圓級構裝的分類

晶圓晶方級尺度型封裝技術的設計理念，首要為增加元件與底材之間的距離，亦即選用更大的錫鉛球來進行電性導通。幾乎大部分現有的WL-CSP技術，均採用重分布技術來進行錫鉛球的間距加大，以達成加大錫鉛球體積需求，進而降低並承受來自於基板與元件間因熱膨脹差異產生的應力，增加元件的可靠性。

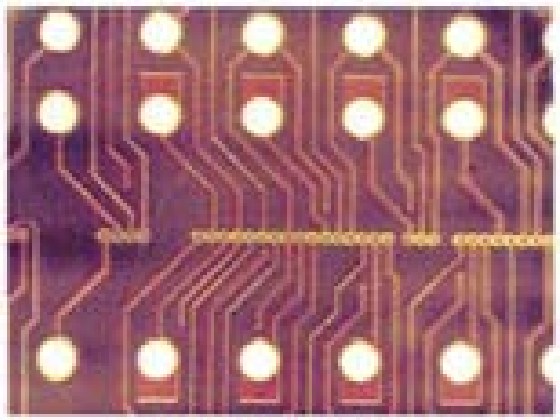
1.重分佈技術(RDL:Redistribution technique)

現有的IC設計仍將鋁墊擺放於die的四周，利用重分布技術可將現有的IC設計，由周邊的鋁墊(peripheral pads)重新設計成矩陣式排列(area array pad)

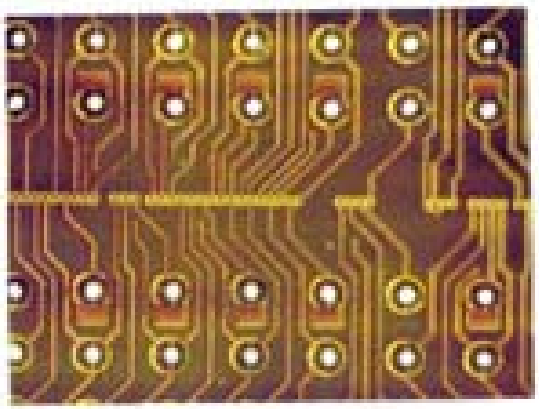
2.利用金球或金凸塊來進行連結

採用金線來替代原有的錫鉛球，此類技術目的在於金屬線具有較錫鉛球更佳的應力緩衝效果，可藉此吸收並減緩晶元與基材之間的熱膨脹差異所產生的應力。最具代表性的則是由Formfactor公司所研發的微探針技術(MicroSpring)

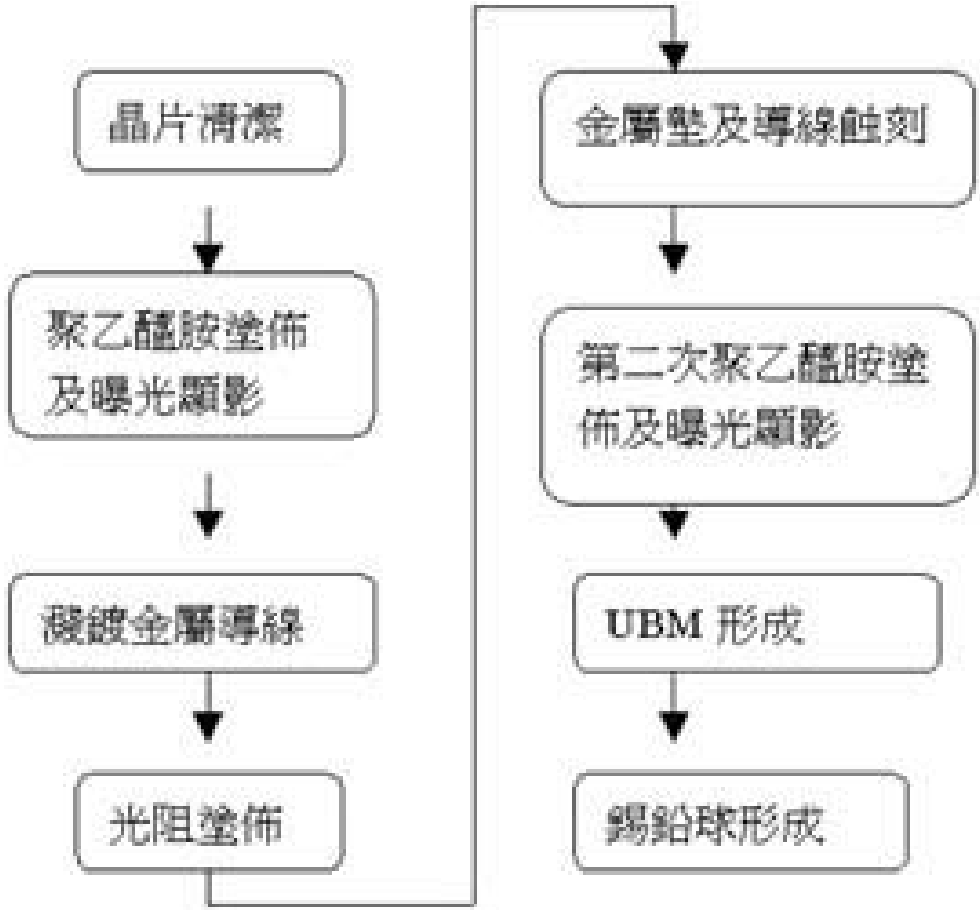
晶圓級晶方尺度型構裝重分布技術製程流程



重分佈後/植球前



已植球



資料來源：APA No. 5, 2002

傳統IC封裝與WLCSP之比較

傳統IC封裝	WLCSP
晶圓先測試，切割	晶圓直接封裝
IC由封裝廠封裝	IC可在fab內封裝或由封裝廠封裝
一次一個IC封裝	一次整片晶圓封裝
在socket進行Burn in	在晶圓直接Burn in
電源及接地在PCB	電源及接地在接合結構中
I/O數目無法降低	具有降低I/O數目的可能性
所有功能設計在IC上	功能可設計分佈在IC及構裝
需要較複雜之底材	有機會選用較簡單之底材
需考慮導線電感	幾乎不需考慮導線電感

資料來源： APA, No. 5,2002

各家公司之晶圓級晶方尺度型構裝結構比較表

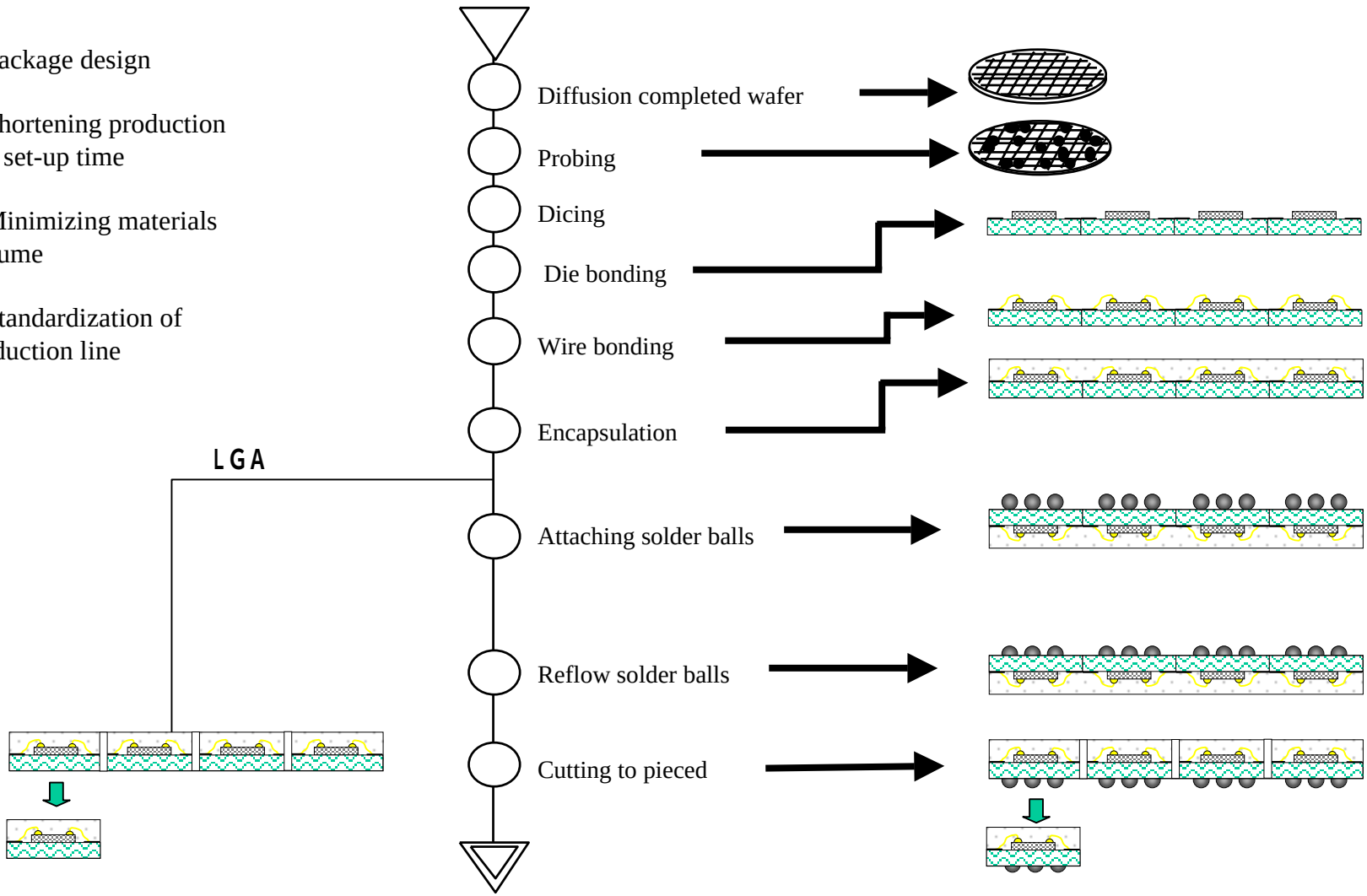
綫線方式	晶圓級晶方尺度型構裝	介電層	Trace;UBM
Redistribution	EPS / APTOS WL-CSP	2 layer PI	Ti / Cu / Ni Ti / Cu
	EPIC WL-CSP	2 layer PI	Plated Cu Cu / Ni / Au
	Flip Chip Technologies?UltraCSP	2 layer BCB	Al / NiV / Cu
	Fujitsu SuperCSP (SCSP)	1 PI 1 EMC	Ti / Ni / Cu Cu post / Ni
	Sandia National Laboratories Mini Ball Grid Array Package (mBGA)	2 BCB	Ti / W / Ni / Cu TiW / Cu
	Mitsubishi CSP	1 PI 1 EMC	TiN / Ni / Au
	Hyundai Omega-CSP	1 SBL 1 BCB	Ti / Ni / Cu
	Toshiba CSP	2 PI	
	Oki / Casio WLCSP	PI or BCB	Copper post
金線連接	FormFactor MOST		Gold wire
可撓性軟板	Amkor wsCSP		Gold wire
	Tessera WAVE	1 elastomer	Cu / gold wir
玻璃基板	ShellCase Shell-PACK / BGA		Ni / Au

資料來源：
APA, No. 5,2002

Assembly flow of matrix BGA/LGA

Source:Casio

- Package design
- Shortening production line set-up time
- Minimizing materials Volume
- Standardization of production line



WL-CSP面臨的挑戰

元件的縮小化(Die shrink)

根據Moore Law，每18個月IC上的電晶體數目就會加倍，若將此對應到元件構裝上則將造成元件尺寸的縮小化，以晶圓級晶方尺度構裝原有的設計也將因此而面臨挑戰。

價格

晶圓級晶方尺度構裝必須在價格上與傳統的CSP或TSOP相近，甚至需要更便宜，此價格的目標為1cent / pin。因此，晶圓尺寸的加大、WLCSP架構、量產可行性、材料選擇均十分重要；另外，由於所有的製程均在晶圓上完成，因此產率的提昇，將扮演最重要的價格因素，及最終能否成功的關鍵。

可靠度

由於晶元與底材之間的熱膨脹係數差異，造成可靠度的下降。因此錫鉛球的大小、錫鉛球的熱疲勞性質以及應力緩衝層的設計與運用等，將影響最終的可靠度。以目前現有的許多晶圓級晶方尺度構裝架構來看，對於較小的晶片應可提供足夠的需求，但對於較大的晶片則仍需努力。

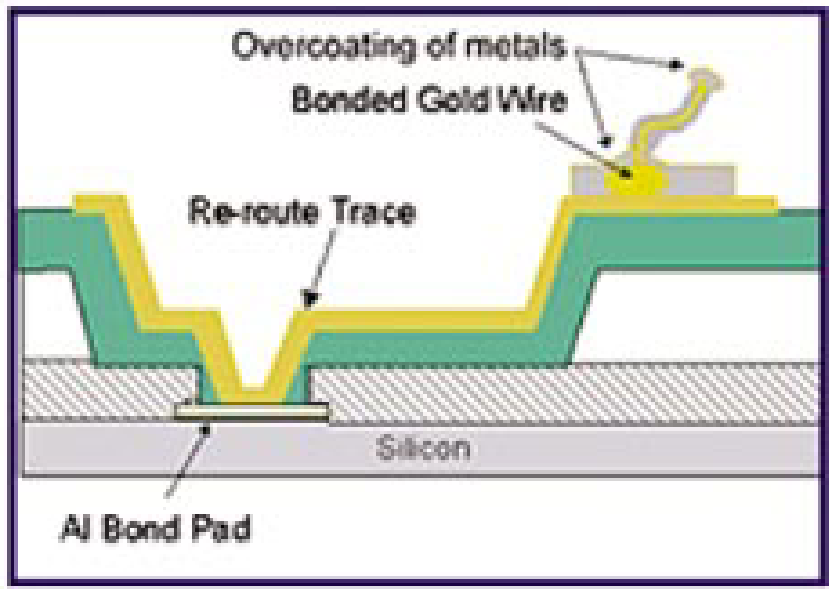
測試方法(Wafer level testing)

KGD的價格目標必須要與TSOP的價格相近似，也就是必須要低於0.01cent / pin。針對WLCSP測試部分必須面臨的問題，首先是尋求具有應用價值的晶圓級Burn-in (WLBI)系統，需考量高密度接觸點、熱膨脹差異、接觸點共平面性、接觸點壓力等；其次，尋求自動化晶圓檢測及電性測試；最後則需考慮價格 / 效能比，此為最終成敗的關鍵。

資料來源： APA, No. 5,2002

利用金球或金凸塊來進行連結

FormFactor公司的晶圓級晶方尺度構裝

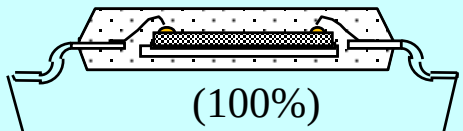


資料來源：FormFactor

Characteristics of WLCSP

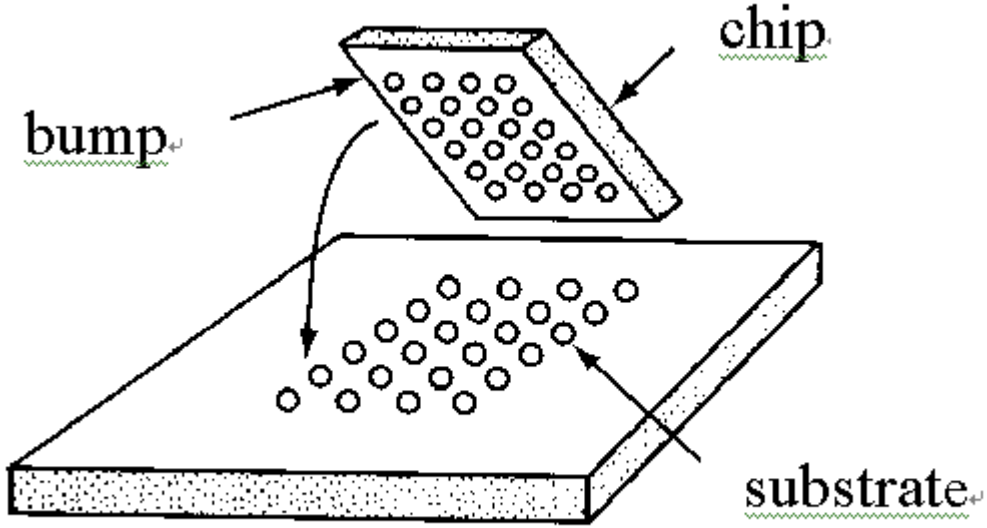
- An LSI package equivalent to a chip size is realized.
- The lightest LSI package is realized.

The most suitable LSI packages for personal and mobile applications

Package type	Size comparison (example)	Weight(g)
Fine pitch QFP	 (100%)	0.60
Fine pitch BGA	 (50%)	0.30
Wafer-level CSP	 (25%)	0.07

Flip Chip Technology

IBM在1960年代即發展出被喻為FC封裝始祖的C4（Control Collapse Chip Connection）技術。



資料來源： Digitimes,

FC 簡介

- FC封裝係將晶蕊倒置，透過精密對位及貼合技術，將晶蕊上已作好之錫鉛凸塊（Solder Bump），在熱融後接合於底層陶瓷印刷電路板上。由於晶粒接點與承載基板面對面接合，改善傳統打線接合（Wire Bonding）封裝體積過大之缺點，加以毋須經過模封步驟(Molding)，晶粒背面裸露提供更佳散熱效果。尤其FC封裝所提供之I／O數是目前所知最高者，已能達到1,500點以上，可充分因應現今電子產品講究高效能、輕薄短小的趨勢。
- 更具體地陳速，當電子產品功能日益強悍，而電壓卻被要求降低時，IC設計人員便面臨了**如何控管晶片內晶體耗電量，及解決電磁相容（EMC）與電磁干擾（EMI）等問題**，這時唯有以一有效封裝降低元件互連間耗損及電感（Parasitic Inductance）才能解決，而FC封裝憑藉SMT（Surface Mount Technology）製程，得以容納更多I／O數及降低電磁干擾，且因裸背得以在產品發熱特性過大時，於背部加裝金屬散熱片，就當前各類封裝來看，實難以找到具備同樣優勢者，直截地說，FC封裝勢必成為未來IC封裝的主要解決方案。

High Performance Requirements

- 半導體走向銅製程，及系統單晶片（SOC）挾整合優勢成未來IC發展趨勢，將有助於進一步推動FC封裝市場的擴張。由於銅製程可將大量功能整合於單一晶片上，在訊號I／O數上雖然會收到減少的效果，但由於晶片複雜度提升，內部晶體數隨之增加，反造成傳遞功率之I／O數擴增，故整體而言，I／O數將有增無減。SOC產品亦對電性干擾與高I／O數等問題十分注重。
- 在二者對電氣特性與I／O數極大要求下，FC技術恰可從封裝角度上提供最適宜之解決方案。
- 以300pin設計的IC封裝為例，在面積比較上，QFP比BGA（非與FC搭配之單純BGA封裝）比TAB比FC是10：5：4：2，若是重量比較，則比例更放大至20：10：8：1，顯示FC在封裝上具備極大優勢，是各方看好的主因。上述比較雖然涉及不同封裝所使用基板材質、封裝材料亦可能不同等基準不一問題，但就封裝概念來看，特定封裝使用特定板材本就無可厚非，故此比較價值仍可成立。

Flip Chip Packaging: FCIP vs FCOB

- 從完整的電子構裝結構來看，FC封裝被歸類在1　1.5層級構裝，係以封裝形式劃分。目前市場上對FC封裝產品約略區分成FCIP（Flip Chip in Package）與FCOB（Flip Chip on Board）二種。前者在技術上包含晶粒凸塊製作、結構設計和原件整體構裝，常與CSP、BGA配合使用，概念上接近元件，是屬1級構裝。後者僅涵蓋將晶蕊倒置，直接接合於下層載體（Carrier）這道製程，為1.5級構裝。
- 二者目前在市場上分別有各自領域，FCIP主瞄準高階市場，如CPU、特殊IC等，而FCOB則以打低階產品為主，多是考量成本、輕量化等因素，產品利潤雖相對較低，但市場規模卻較FCIP大上許多。雖然FCIP目前多為高階IC所採用，但就長期來看，為直接置晶（DCA:Direct Chip Attachment）的FCOB才是真正趨勢所在。

資料來源： Digitimes,

FCOB一大趨所勢　唯技術面仍待努力

- 技術問題是當前FCOB不易走向高階產品的一大關鍵。由於製程中省略載體，直接面對了下層基板，當核心元素晶蕊具備較高集積度與I／O設計時，缺少了上層IC載板的接合基板在線路設計上勢必更加複雜，及難以製作，因之中有些製程涉及半導體。而這裡必須強調的是，當前市場上指陳的FC封裝產品多半是圍繞在FCIP上。
- Flip-Chip封裝是Intel的大刀:前段晶圓廠的製程不是晶片組發展的瓶頸而在頻率越快、腳數越多的發展趨勢下，封裝反而是晶片組在製程技術上發展的關鍵，傳統打金線封裝在頻率不斷提升下，產生嚴重的電感效應，將干擾晶片的電性。Intel在Flip-Chip封裝上佔有極大優勢，從Pentium II 開始，Intel就採用Flip-Chip封裝，緊接著晶片組中的北橋也跟進，Intel擁有成熟的錫鉛凸塊技術、FC封裝技術，更掌握FC載板的材料及技術專利。其他晶片組廠要採用FC封裝，首先面臨問題是FC載板的價格居高不下，使得晶片組的成本暴漲，市場售價低於Intel的策略將難以維持。

資料來源： Digitimes,

Cost Comparison FC vs WB
excl. 覆晶載板

DigiTimes

打線封裝與覆晶封裝製作成本約略比較 單位：美元

Wire Bonding		Flip Chip	
Die Attach & Cure	$0.03	Pick & Place	$0.05
Wire Bonding	$0.23	Bumping Cost	$0.37
Wire	$0.43	Reflow Bumps	$0.05
Encapsulation	$0.10	Clean	$0.01
		Underfill	$0.10
Comparison	$0.79		$0.58

資料來源：零組件雜誌，2008 製表：康智超、柯博偉

在技術層次上，是否必須揚棄打金線封裝，而採用FC封裝，目前還說不定，完全端看設計技術與封裝廠的能力，而且只要一家廠商能夠成功做出打金線封裝的晶片組，其他廠商必定跟進，因為一顆35mm×35mm的6層BGA基板只要1美元，與FC載板價格相差好幾倍，降低成本是最重要的考慮因素。

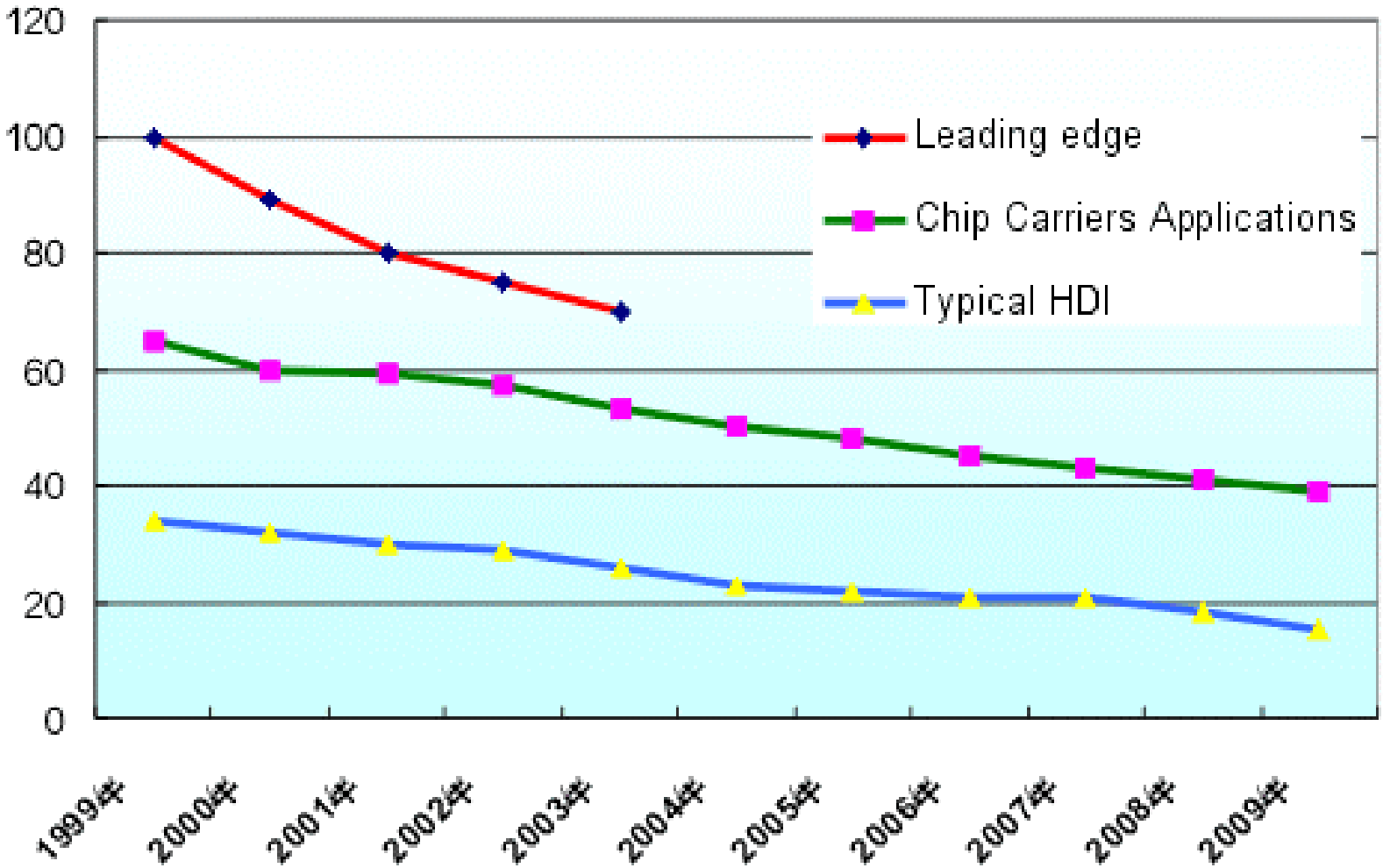
資料來源： Digitimes

覆晶載板 (Flip Chip Substrate)

- FC基板亦屬IC載板的一類，而IC載板在製作上和一般PCB有共通點，早在數年前國內廠商察覺到IC載板商機時，即已陸續投入研發，或透過技轉取得技術，故目前在技術進程上已有一定水準，現階段包括繪圖卡等高階覆晶封裝訂單，都陸續由日月光與矽品取得，在就近供給原物料的前提下，在上游客戶多將訂單下於此的地利情勢下，讓台灣覆晶載板需求大增。台灣PCB產業投入覆晶載板(FC基板)發展相較其他地區業者有利。
- FC封裝有三大關鍵要素，1)即KGD (Known Good Die) KGD的良莠與否直接影響到封裝良率的成敗 ，2)價格是制限FC封裝市場的另一關鍵因素，當中尤以基板及凸塊佔了相當大比重， 3)等待需求面成熟是衡量FC封裝何時成主流的關鍵。
- 載板的採購成本除將影響業者的獲利空間外，亦將成為FC封測廠未來競爭的決戰關鍵點。

高階PCB未來線幅走勢

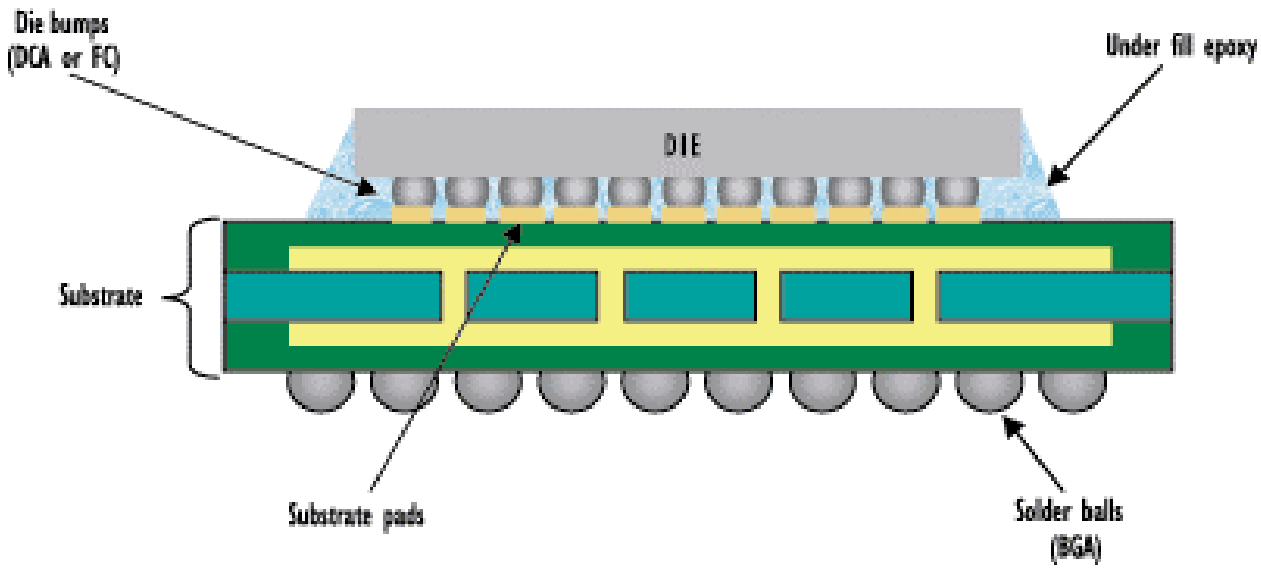
單位：μm



What is Flip Chip ?

- Flip chip microelectronic assembly is the direct electrical connection of face-down (hence, "flipped") electronic components onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip bond pads. In contrast, wire bonding, the older technology which flip chip is replacing, uses face-up chips with a wire connection to each pad.

Pictorial Of A Basic Flip Chip Package:



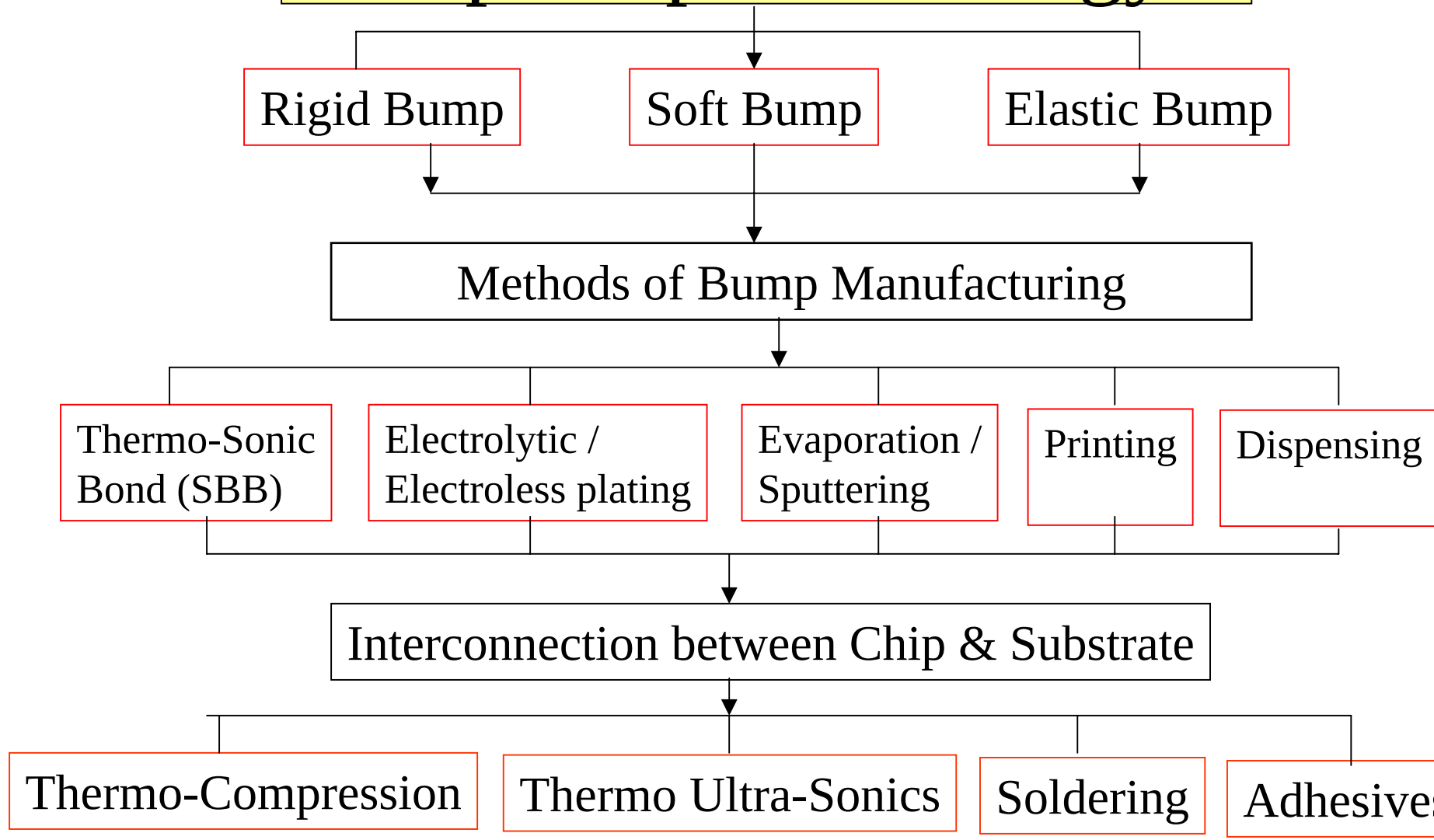
Why Use Flip Chip?

- The boom in flip chip packaging results both from flip chip's advantages in size, performance, flexibility, reliability, and cost over other packaging methods and from the widening availability of flip chip materials, equipment, and services.
- Smaller Size: Eliminating packages and bond wires reduces the required board area by up to 95%, and requires far less height. Weight can be less than 5% of packaged device weight. Flip chip is the simplest minimal package, smaller than Chip Scale Packages (CSP) because it is chip size.
- Highest Performance offers the highest speed electrical performance of any assembly method. Eliminating bond wires reduces the delaying inductance and capacitance of the connection by a factor of 10, and shortens the path by a factor of 25 to 100.
- Greatest I/O Flexibility Flip chip gives the greatest input/output connection flexibility. Wire bond connections are limited to the perimeter of the die, driving die sizes up as the number of connections increases. Flip chip connections can use the whole area of the die, accommodating many more connections on a smaller die.

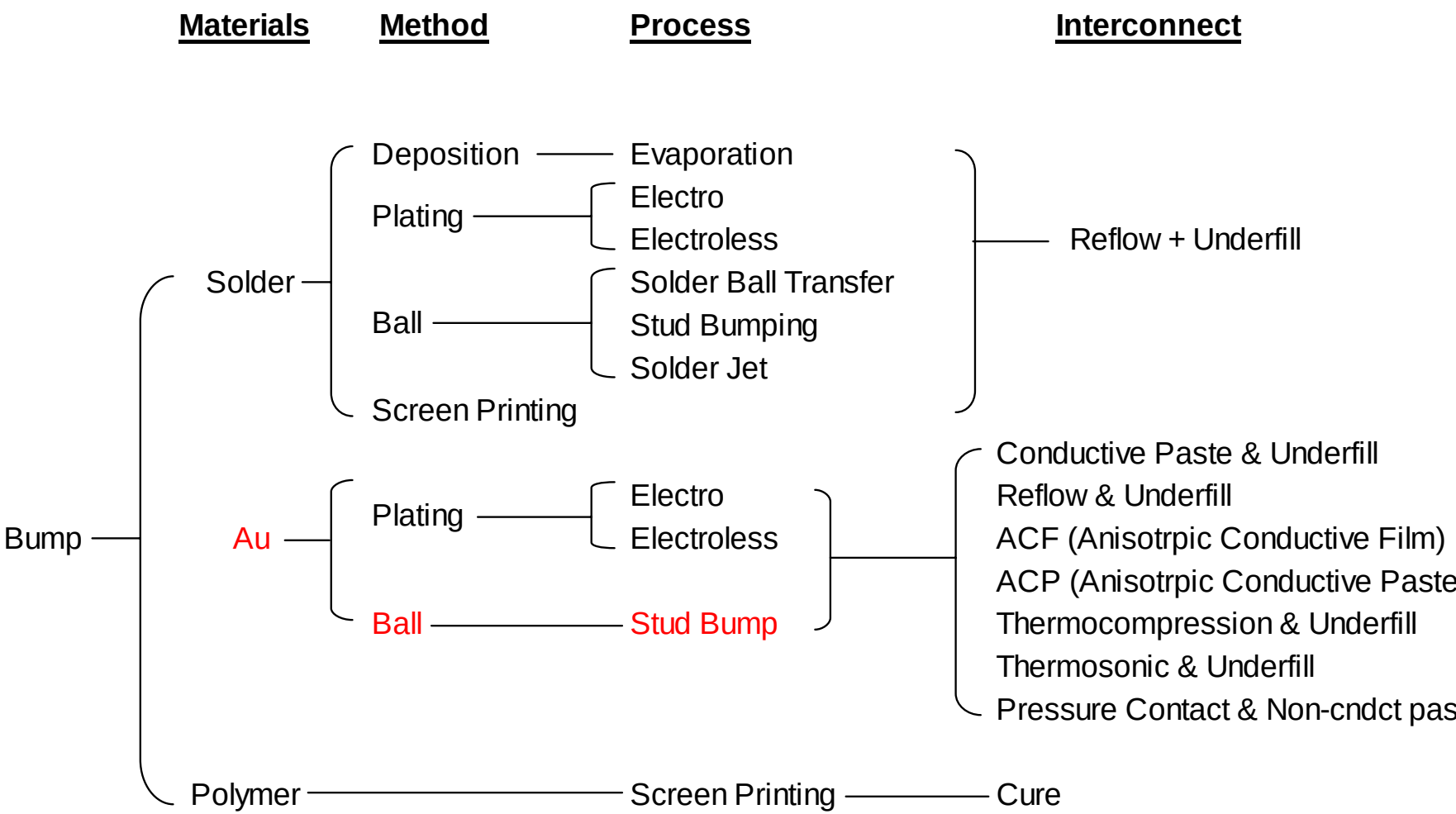
Why Underfill ?

- The underfill protects the bumps from moisture or other environmental hazards, and provides additional mechanical strength to the assembly. However, its most important purpose is to compensate for any thermal expansion difference between the chip and the substrate. Underfill mechanically "locks together" chip and substrate so that differences in thermal expansion do not break or damage the electrical connection of the bumps
- Underfill may be needle-dispensed along the edges of each chip. It is drawn into the under-chip space by **capillary action**, and heat-cured to form a permanent bond.

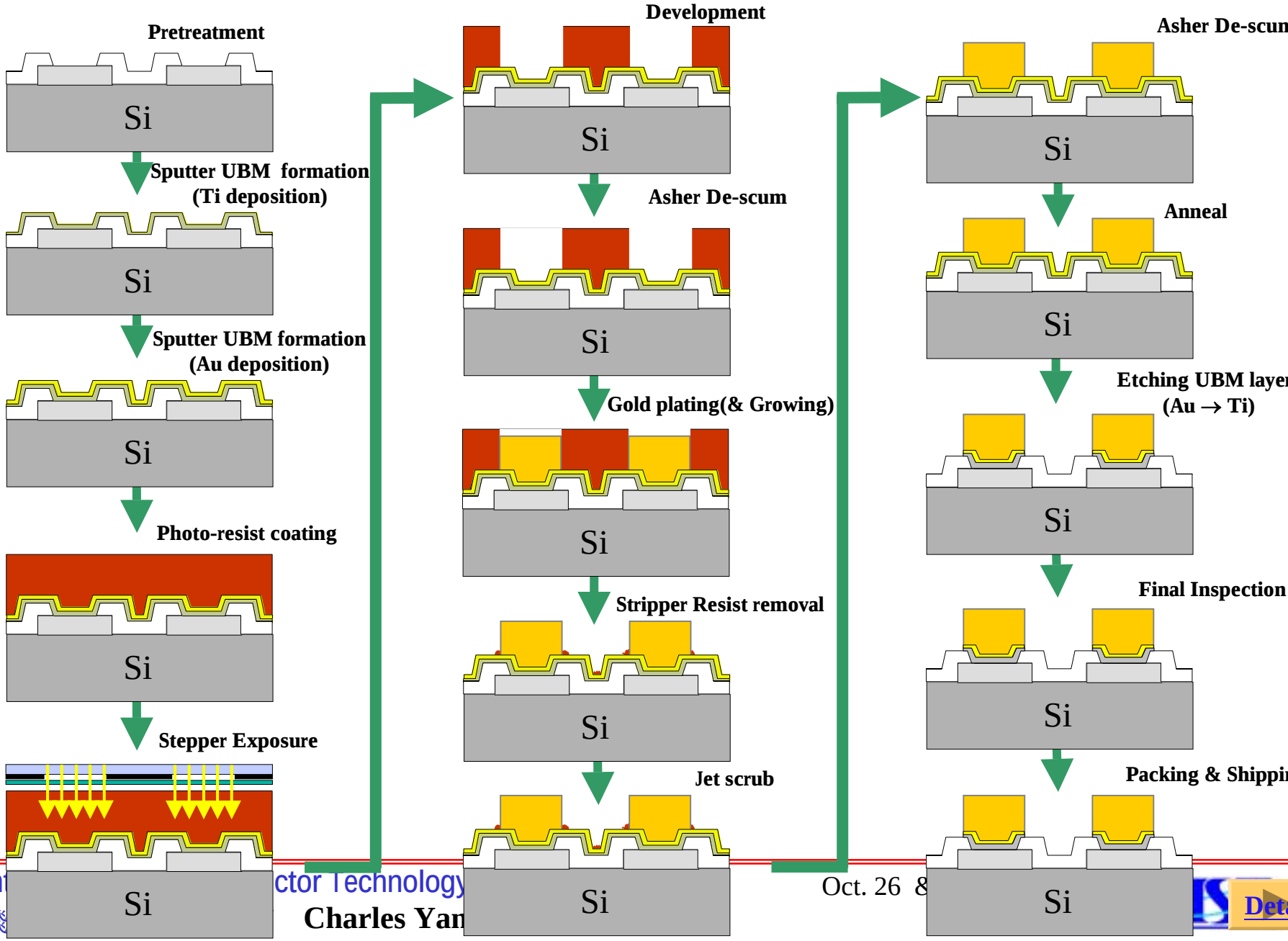
Flip Chip Technology



Bumping for Flip Chip

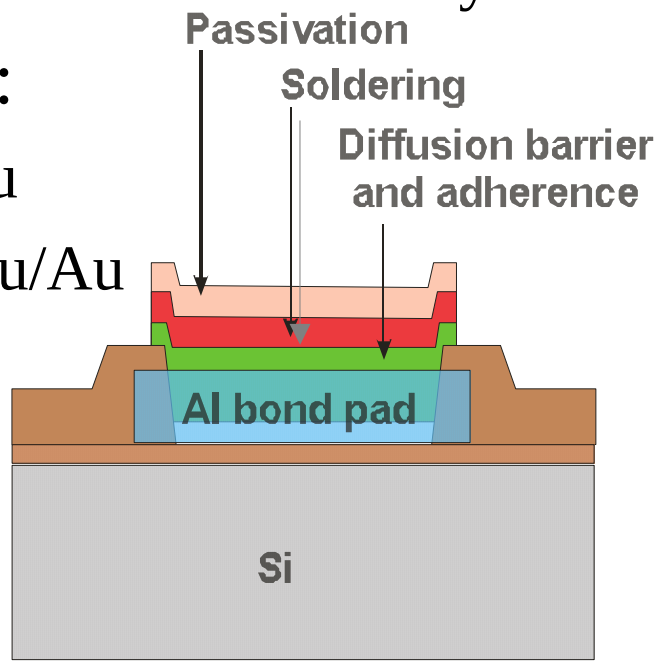


Gold Bump Process Overview



Under Bump Metallization (UBM)

- Aluminum not suitable for direct bump bonding
  - Al_2O_3 passivation layer
  - Au-Al intermetallics
- Process steps (mod. 1)
  - Sputter etching metal layers
  - Normal photolithography
  - Metal etching
- Process steps (mod. 2)
  - Spin on 5 µm photo-resist
  - Sputter etching metal layers
  - Lift off
- Metal layers :
  - 1st: Diffusion barrier and adherence
  - 2nd: Soldering
  - 3rd: Passivation for 2nd layer
- Examples:
  - Ti/Ni/Au
  - Ti/Au/Cu/Au



Requirements of UBM

- Good adhesion to bonding pad metallization and wafer passivation
- Good ohmic contact to bonding pad metallization
- Solser diffusion barrier
- Solder wettable
- Oxidation barrier
- Minimum stress on silicon

UBM Functions

- Adhesion and diffusion barrier layer

  Function: From strong bond with bonding pad metallization and IC passivation layer and prevent diffusion between bonding pad metallization and solder bumps.

  Typical metals used: Chromium (Cr), Titanium (Ti), Titanium/Tungsten (Ti/W), Nickel (Ni), Palladium (Pd), Molybdenum (Mo)

  Typical thickness : 0.15 to 0.2 um

- Solder wettable layer

  Function: Provide surface for solder bump to adhere to.

  Typical metals used: Copper (Cu), Nickel (Ni), Palladium (Pd).

  Typical thickness : 1 to 5 um

- Oxidation barrier layer

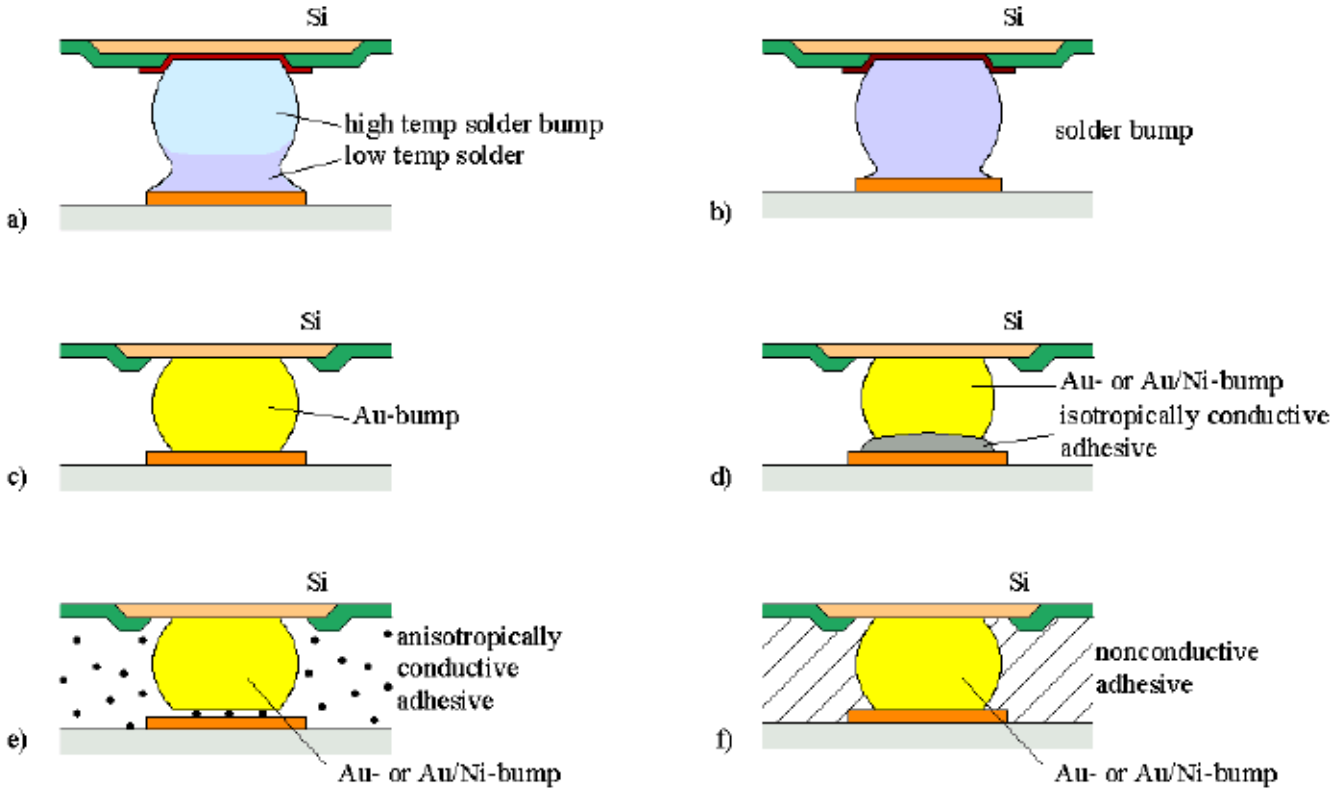
  Function: Prevent UBM structure from oxidation.

  Typical metals used: Gold (Au)

  Typical thickness : 0.05 to 0.1 um

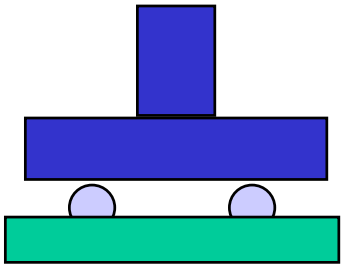
Ti/Cu/Au, Ti/Cu, Ti/Cu/Ni, TiW/Cu/Au, Cr/Cu/Au, Ni/Au, Ti/Ni/Pd, Mo/Pd

Various Flip Chip joints vs Bonding pressure/temperature

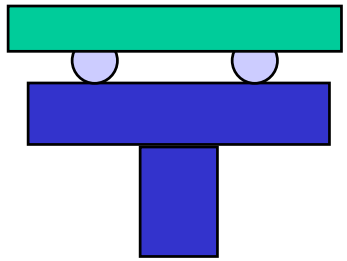


	joints	op pressure	op temperature	remark
a)	high lead	very low		solder reflow
b)	eutectic solder	very low		solder reflow
c)	gold to gold	60 g/ bump	>200 deg C	ultrasonic, stud bump
d)	conductive glue	very low	< 200 deg C	suitable stud bump
e)	ACP/ACF	100 g/bump	200 degC	Pressure cure
f)	NCP	Medium		Pressure cure, stud bump

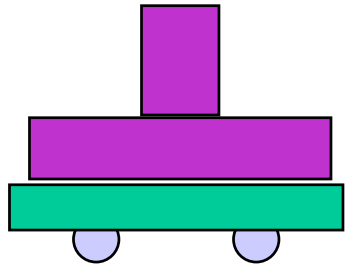
Flip Chip (Soldering / C4) Process Steps



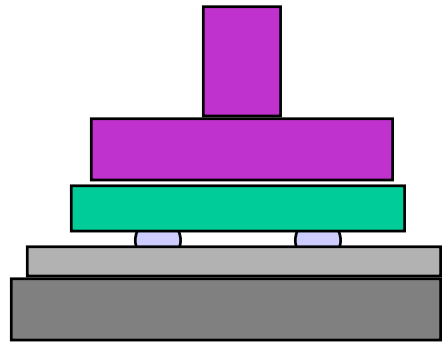
Pick from Wafer



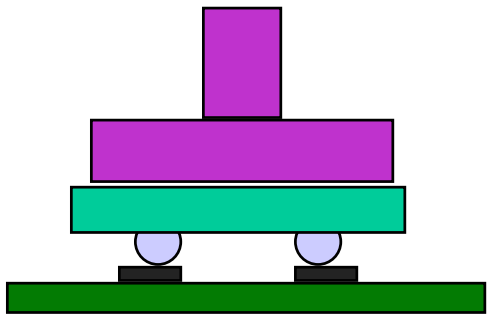
Flip



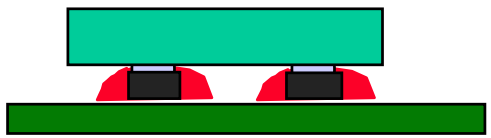
Pick from Wafer Handler



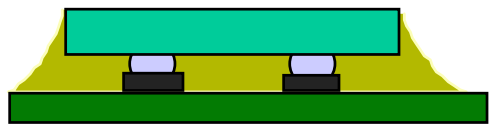
Dip in Flux



Vision and place



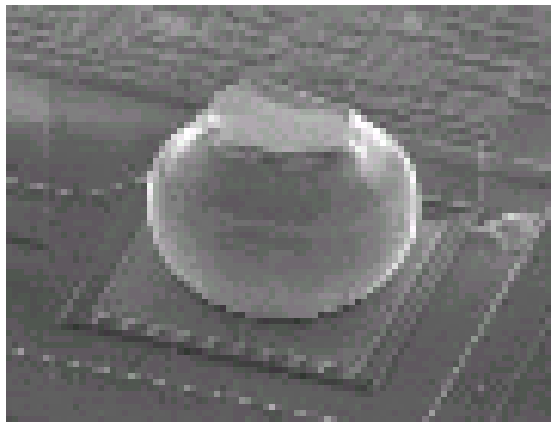
Reflow



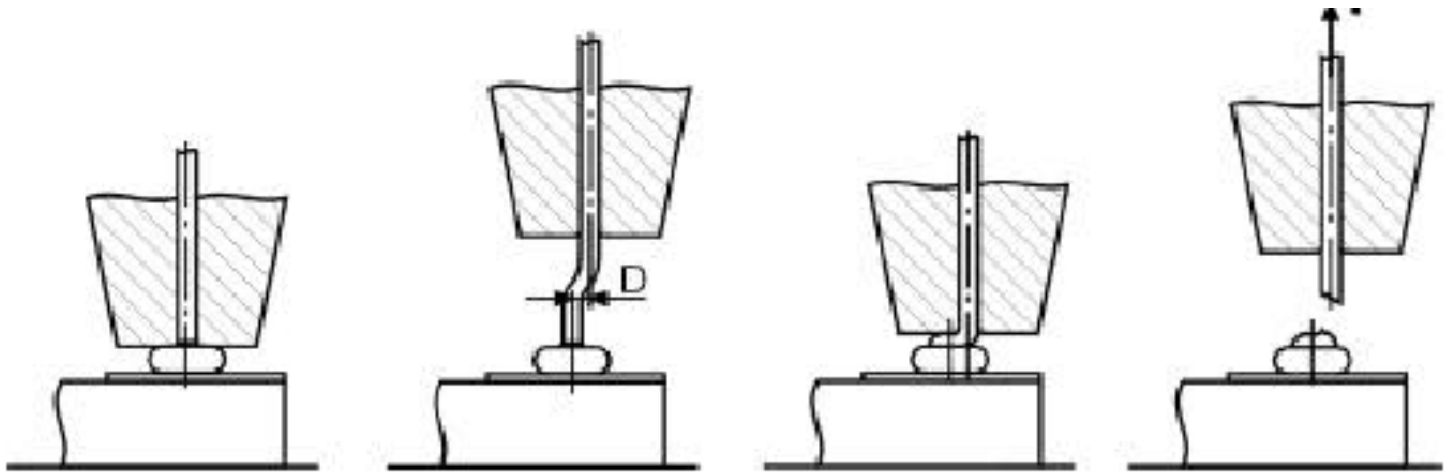
Underfilling and curing

Stud Bump Formation

- Stud Bump formation: ESEC wire bonder



Gold wire : 1% Pd, 30 um dia.
Capillary : use current one
Design a vacuum heat block
with single chip manual load/unload



Electroless UBM Process Flow

Under Bump Metal Process

Electroless Plating of Ni/Au Bumps

Backside Coating

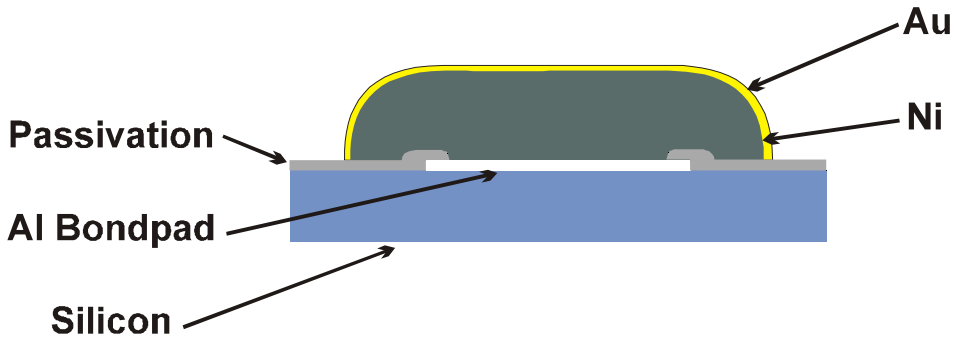
Aluminum Cleaner

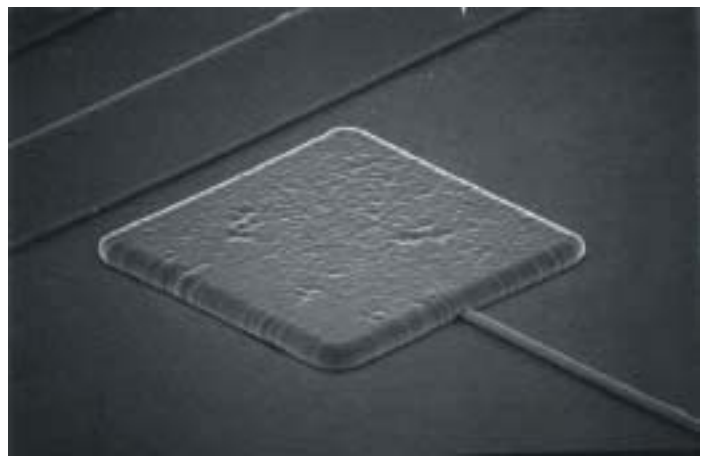
Zincate Pretreatment

Electroless Nickel Bath

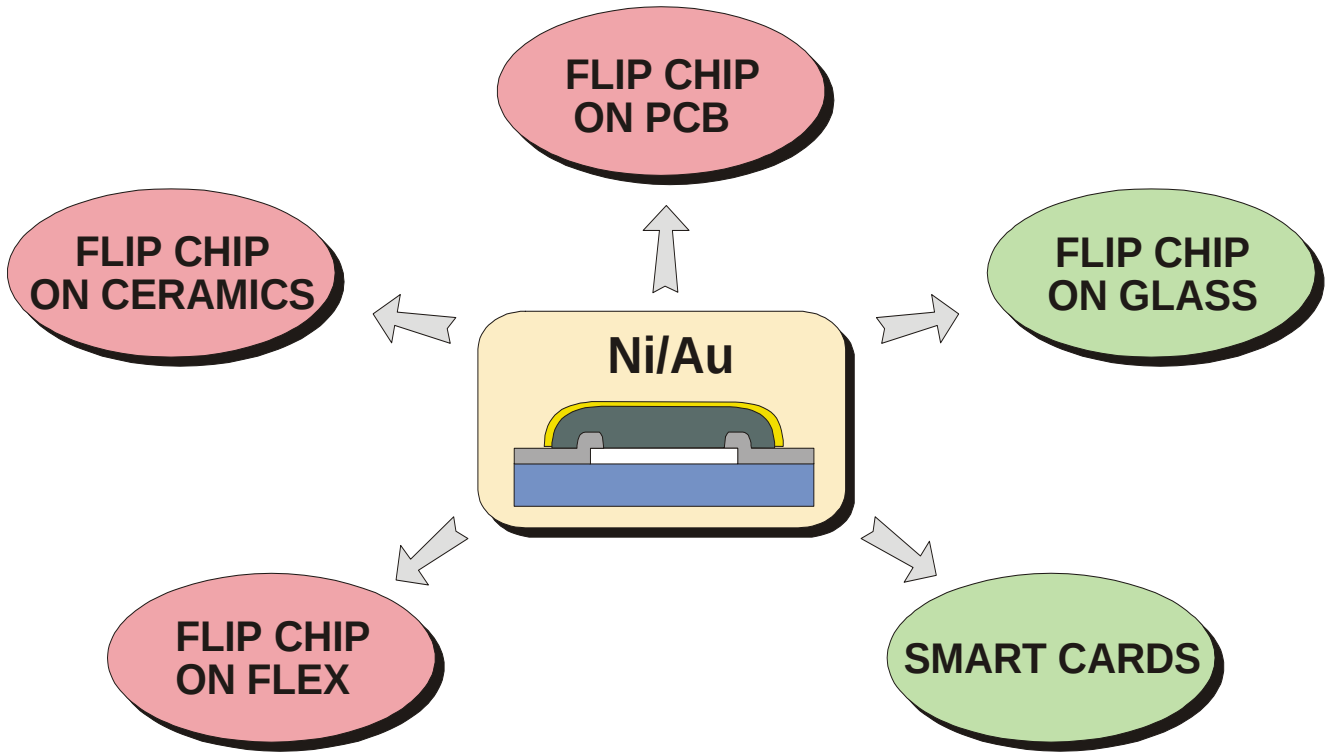
Immersion Gold Bath

Coating Removal





Electroless Under Bump Metallization for Flip Chip Applications

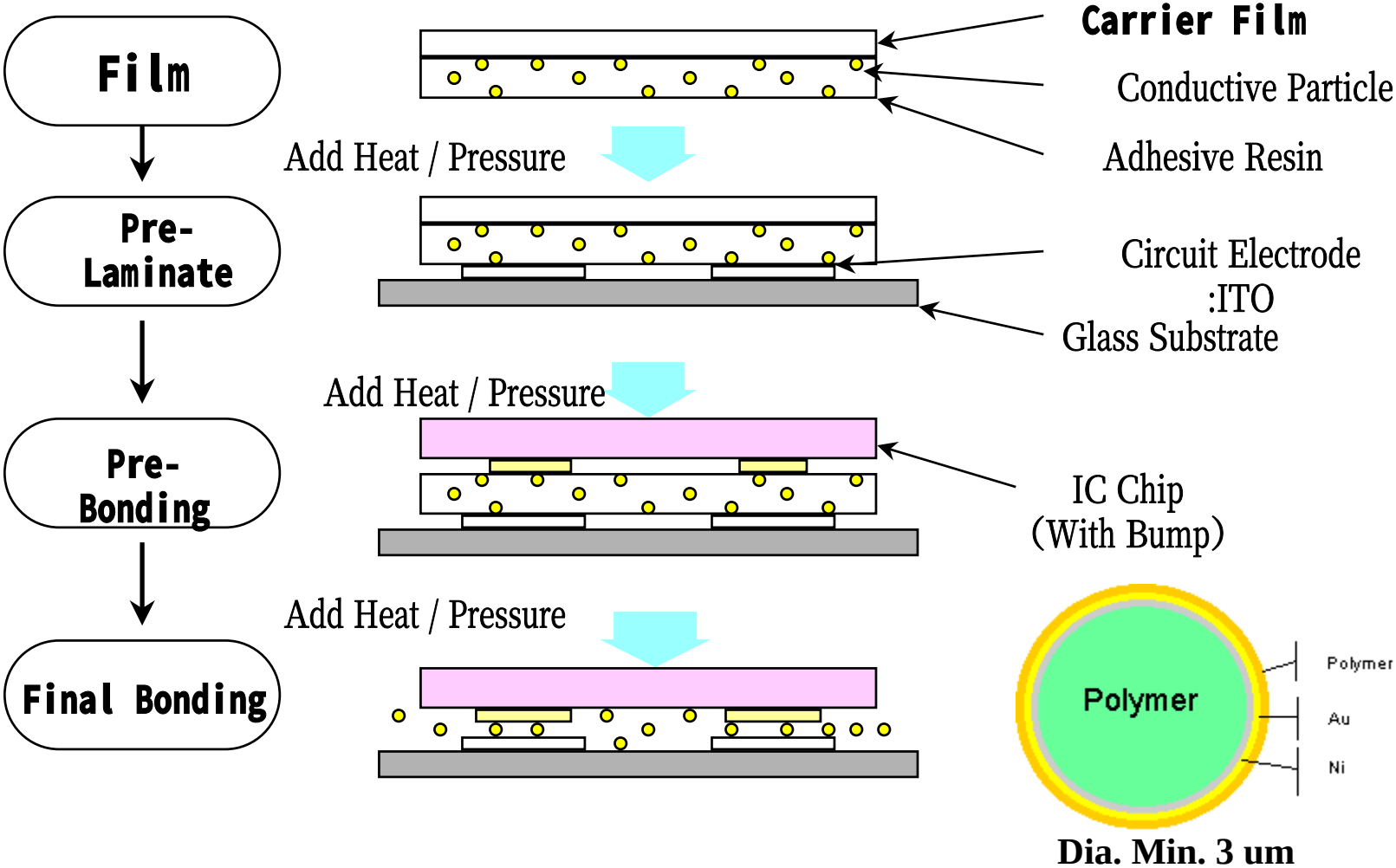


Bump Technology Comparison

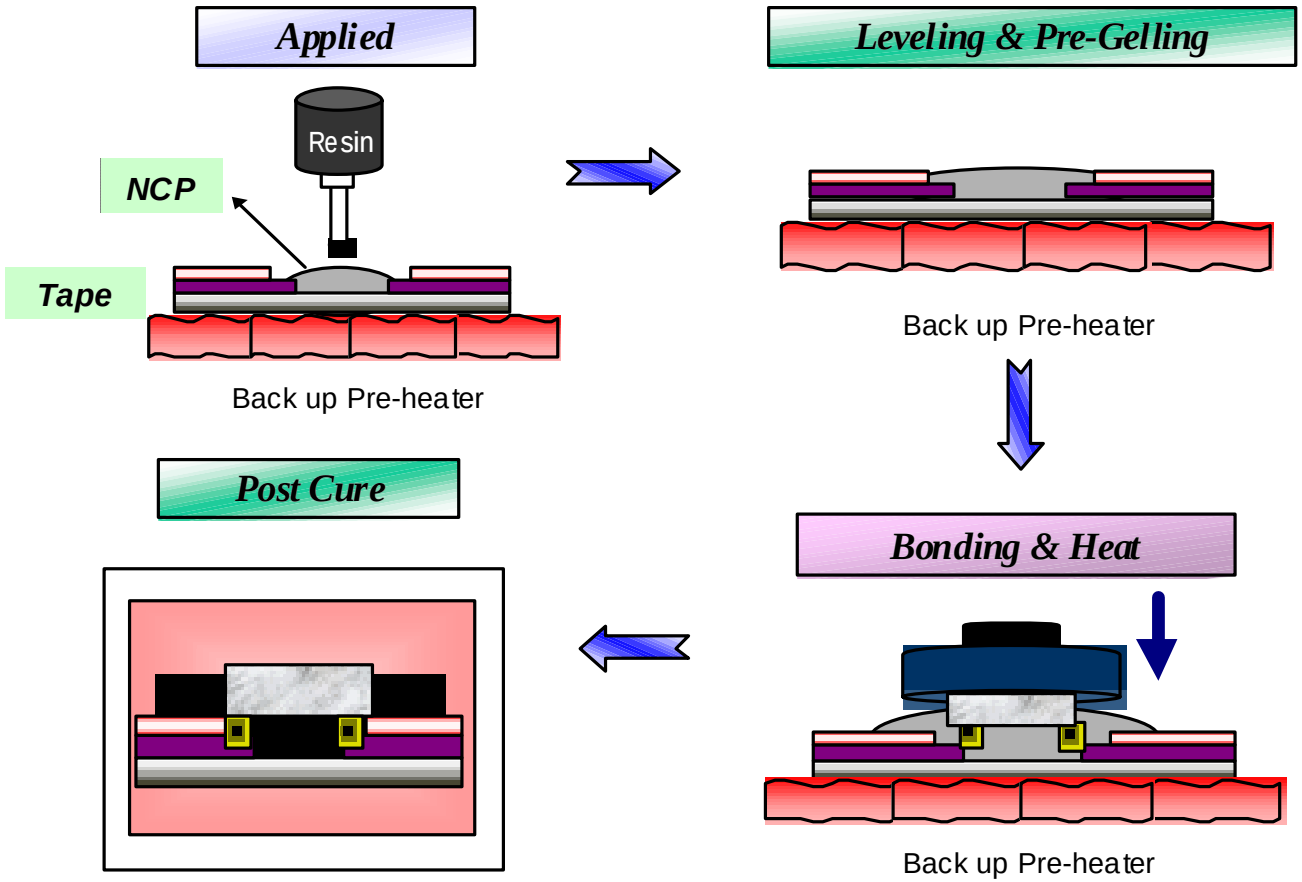
	Min. ball size	Min. Pitch	Bump material	UBM	Substrate	Comments
Evaporation through mask	100 µm	250 µm	Pb/Sn	Cr-Cu	Wafer	No fine pitch
Screen printing	100 µm	200 µm	Pb/Sn Sn/Ag/Cu	Ti-Ni-Au	Wafer	Most widespread Cheap
Stud bumping (SBB)	70 µm	45 µm	Au Pb/Sn	No need	Wafer Chip	Low throughput No self-alignment
Electroplating	25 µm	40 µm	Pb/Sn Cu/Sb/Ag/Sn	Cr-Cu TiW-Cu-Au Ti-Ni-Au	Wafer	Need for tight control
Electroless plating	40 µm	70 µm	Ni/Au	Zn	Wafer Chip	Need for pad conditioning
Conductive Polymer Bumps	100 µm	150 µm	Polymer	Cr-Au	Wafer	Very new High Rc

Pb alloys can be alfa sources

Process Anisotropic Conductive Film (ACF) COG



NCP Process Flow



Source: Namics Corp.

Equipment: Shinkawa COF-110

填膠技術 (Underfill dispensing)

(1) 點膠機台

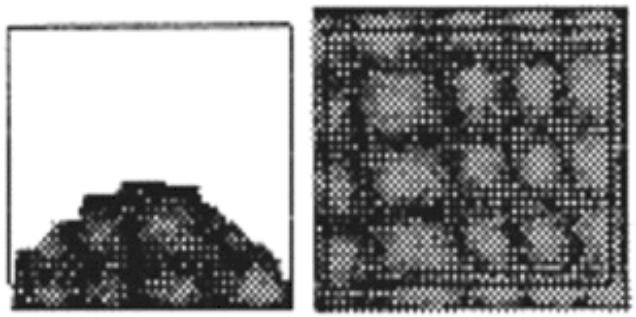
加熱系統：溫度要穩定誤差小，溫度控制誤差±5°C以下。基板要平貼在加熱工作台上，使基板均勻受熱。膠量控制：要量化、有監控及校正系統且重現性佳。

(2) 加熱方式：加熱器數量，片狀或條狀均會影響溫度均勻度，工溫度誤差作台面±5°C以下。

(3) 點膠圖形：事先分析點膠路徑選擇一字形、L字形、U字形那一型最適合？

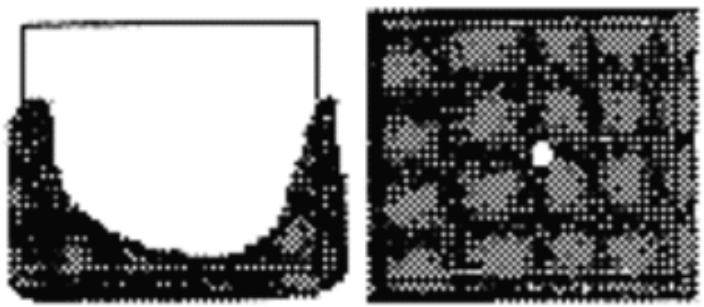
(4) 覆晶填膠製程在全部製程中速度最慢，因為膠材以毛細現象在微小間隙內流動，晶粒尺寸增加要維持良品率是很困難的亦即點膠時間和包覆氣泡的機率相對增加。

各種流動模式流動分析

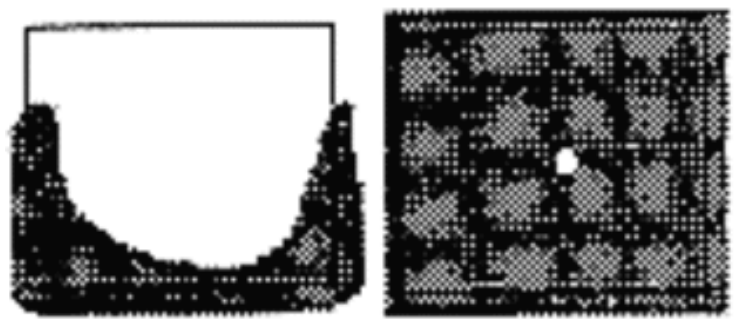


一字形

點膠品質會受到晶粒尺寸、凸塊排列以及密度、接點高度、工作溫度、基板影響，並且發揮膠材特性，另外構裝設計階段即將填膠工程一併考慮，方呈現良好的點膠品質。



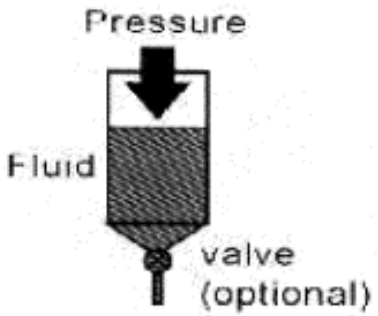
L字形



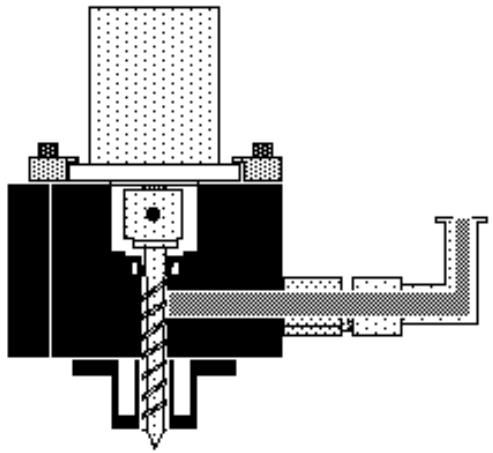
U字形

點膠機點膠閥比較

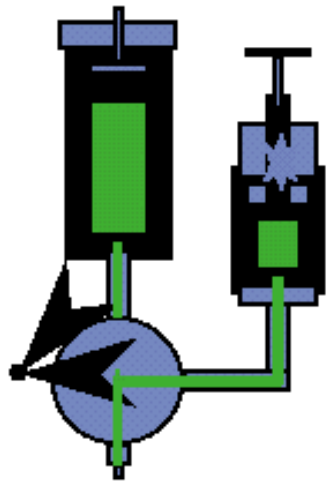
- 如圖所示三種點膠閥；Needle閥：點膠量因膠黏度變化而改變，點膠量重現性＞±10％。Auger閥：點膠量重現性±4％至±10％，點膠量也會因膠黏度變化而改變。LPDP閥：點膠量不會因膠黏度變化，點膠量重現性在20μc.c 以下點膠量 ±1％。



Needle



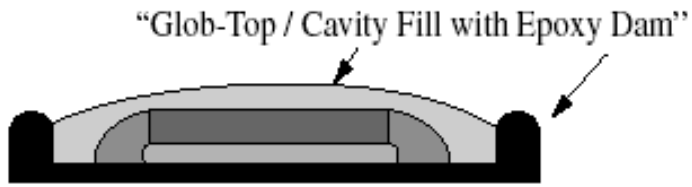
Auger

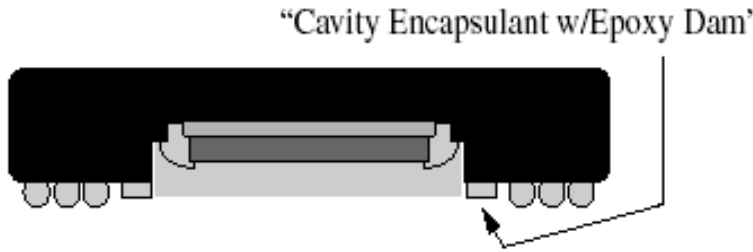


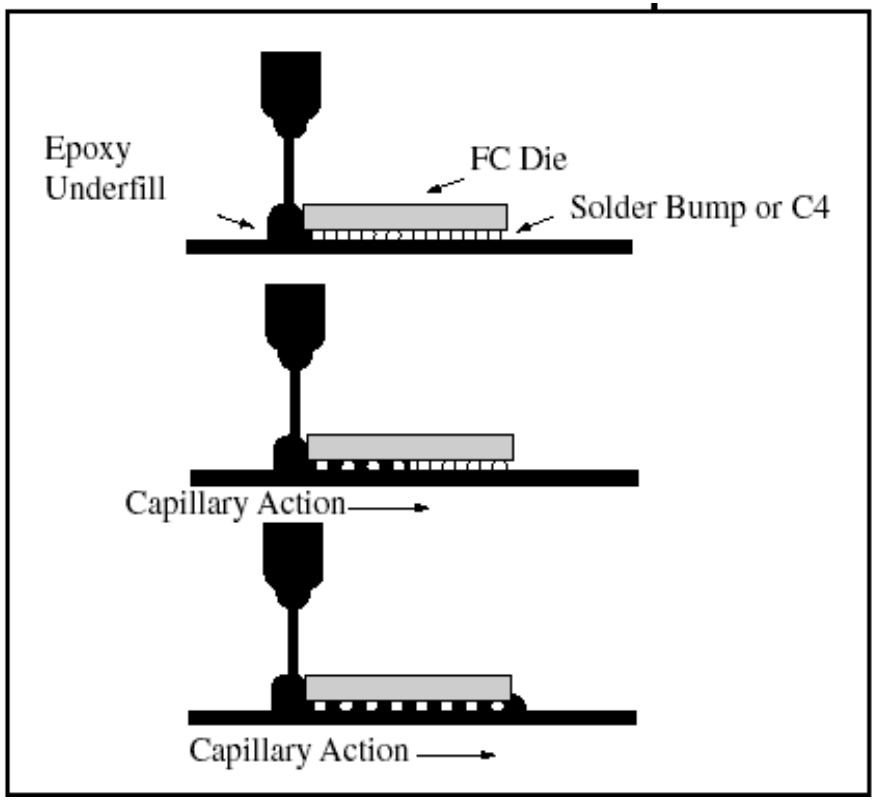
LPDP

Dispensing Liquid Encapsulants

- Glob-top
- Dam & Fill
- Underfill







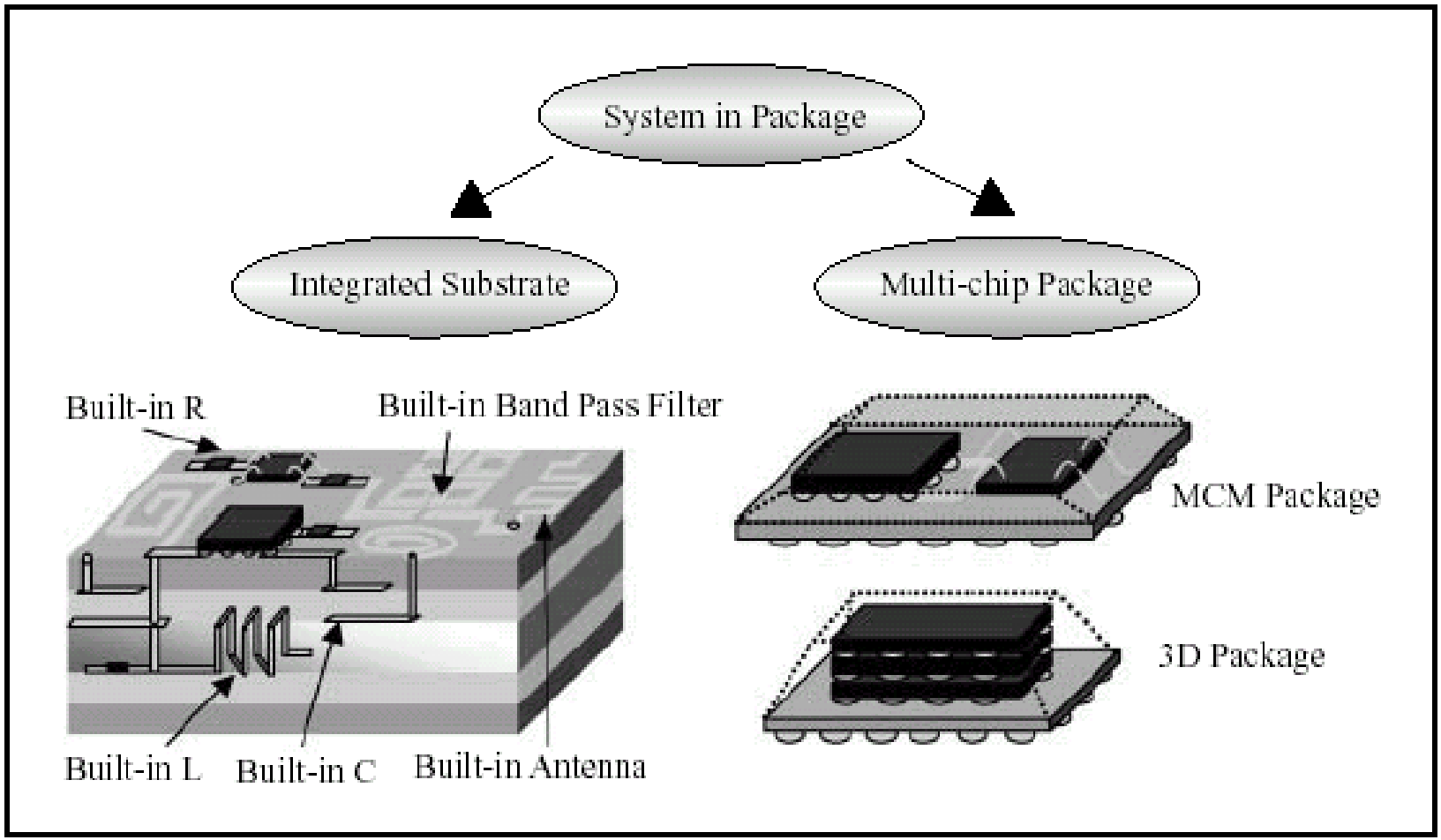
one of function of the bump is to provide a space between the chip and the board. In the final stage of assembly, this under-chip space is usually filled with a non-conductive "underfill" adhesive joining the entire surface of the chip to the substrate, and re-distribute the residual stress from on the interconnection joints to all the chip surface.

SiP / Stacked Chip / MCP

由於可攜式消費性及電腦產品持續的功能提升，使得電子工業OEM廠商必須以較小及較輕形式提供這些產品，乃是一大挑戰；這對於矽元件供應商除了要增加晶片功能，並將晶片裝入一個更小的構裝中來說，是龐大的壓力。最近幾年在單晶片構裝中的顯著進步滿足如此的需求，但是現在壓力持續著，導致更多的焦點集中在將多重晶片放入單一構裝內。

MCP:多重晶片構裝(Multi Chip Packaging，MCP)提供幾項優點，包括增加矽元件密度、降低系統成本及提高可靠度。這些優點帶來許多利益及機會，例如較大的功能積集度、改善板等級(board-level)及系統等級(system-level)的生產良率、較低的能源消耗(較小的電池或更久的電池壽命)，以及較少的與較簡易的保固及專業維修，更不用說簡化的系統設計及模組化。這些利益刺激不間斷的MCP創新。

Scope SiP



Source: 工業材料, Aug. 2003

What is System in Package?

An IC package containing multiple die?

A fully integrated system or sub-system:

- One or more semiconductor chips ***plus***:
- Passive components that would otherwise be integrated on the mother board
  - Surface mount discrete passives
  - Embedded or patterned into substrate
  - Integrated passive components
- Other subsystem components:
  - EMI shield, SAW filters, packaged ICs, connectors, antennas, mechanical housings, etc.
- A fully integrated functional block bridging the gap between SOC and SOB (system on board)

Source: Amkor 2003

Benefits SiP

- Simplify board design and assembly
- Improve electrical performance and interconnection reliability
- Increase functionality per unit area
- Reduce system manufacturing cost
- Flexibility: can make changes to system / sub-system without changing mask-sets or mother board design , combine different fab process product device (ex logic & memory)

多重晶片構裝之優勢Benefits

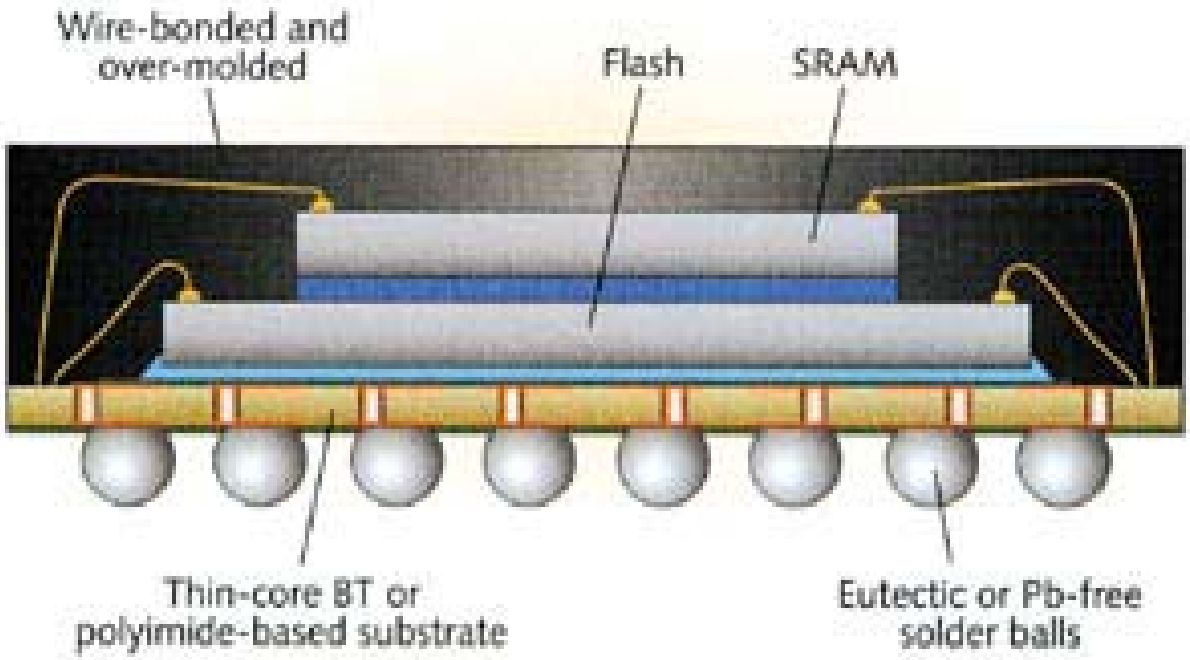
- **加速上市時間(time-to-market)及量產時間（time-to-volume）**。加速產品上市時機起因於在產品層級時，排除任何必要去設計關鍵功能。僅有在一個特定的、標準化的MCP，及其他產品功能之間的界面仍然必須。移除許多原型的故障排除，以及從產品導入周期排除設計問題解決方案，也衝擊到產品量產時間。
- **簡化產品模組化 / 分割，功能提升及模擬**：減少成本仍是任何設計方法最終的價值衡量，且MCP可能以數個方式正面地衝擊成本。最為明顯的衝擊來自於PWB等級，MCP只有在需要時，才將焦點放在模組基材中的高密度連結結構。如此一來，將導致整合的MCP較那些可能直接在印刷電路板上，且有著獨立構裝的集成電路(IC)擁有更大的間距。這些簡化的PWB成本較低且通常產生較高的組裝良率
- **經由簡化印刷電路板(PWB)結構、提高組裝及測試良率，並減少策略支出，以降低系統成本；**
- **改善產品可靠度。**因為模組獲得可以導致實質上的「已知良好功能」(known good functions)， 經由消除個別IC元件之間的缺陷相互影響。PWB組裝良率甚至會進一步增加，如此則可改善最終產品的可靠度，因為最多的早么期失效和邊際效能相互作用(零件之間)都已不存在。

What Application in SiP

- 以應用產品來看SiP的市場，其分佈主要以手機為主力產品。除各類型的PA模組、RF模組外，手機內被動元件的整合，也是非常主要的應用元件。
- 記憶卡:
- CMOS Image Sensor Module (CIS Module)

Stacked Chips

- 最常見的操作如圖所示，由一個晶片位在另一顆晶片上面的晶粒堆疊方式構成。最常見使用晶粒堆疊技術的產品，將一個快閃記憶體(flash memory)及一個低功率的靜態隨機存儲記憶體(SRAM)構裝在一起，支援手持裝置及PDA市場。一般由不同的矽供應商所提供，納入MCP中的快閃記憶體及SRAM，成為一種由快閃記憶體製造商所銷售的產品，主要由於不願意將機密的快閃記憶體測試向量(test vectors)釋出給其他供應商。

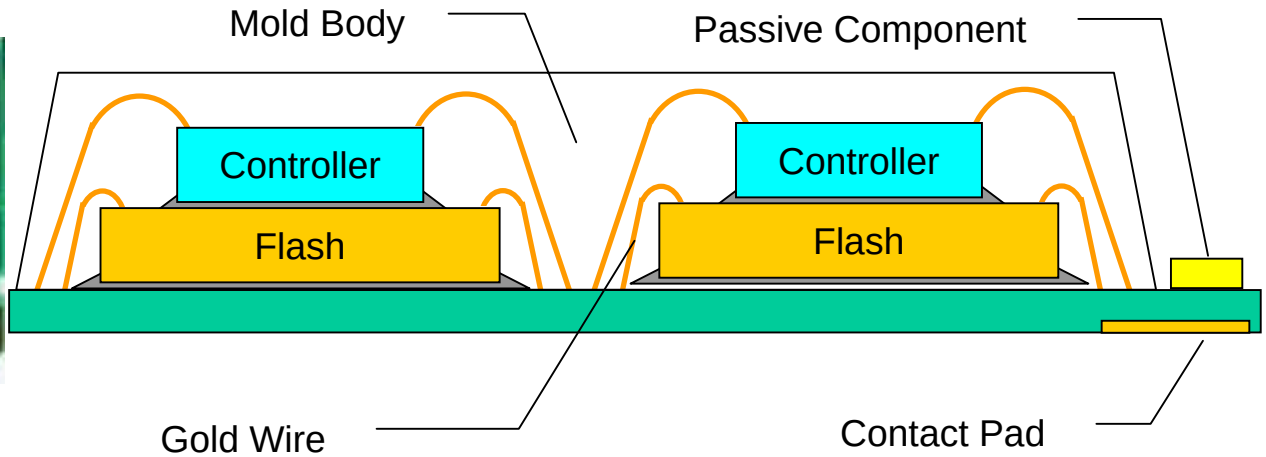


CIS Module & Memory Card

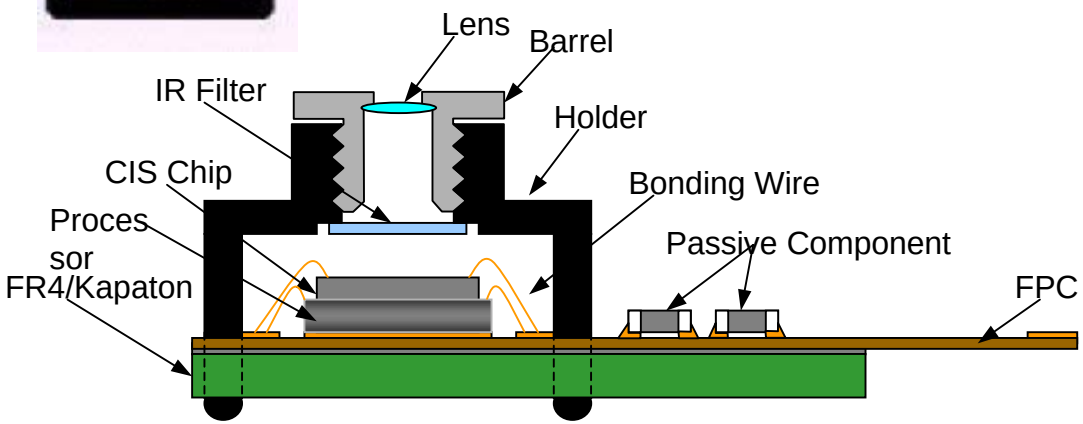
- 隨著對更高精密的構裝整合需求持續增加外，邏輯元件的加入，更驅使了進一步的MCP創新。例如有一種解決方案，需要記憶體才能操作的元件，如數位信號處理器(DSP)或其他微處理器(controller)，與其所需的記憶體，一同放置於一個構裝之中。如此一來，不但可節省空間，而且藉由整合記憶體介面至構裝中，可以減少系統的複雜度。而產生的I/O減少，容許一個較簡單的系統板，且可能消除佈線層與盲孔，並降低系統成本。改進的子系統效能，也是常見的邊際效益，本身在傳統的構裝上很少僅僅只是因為選擇MCP而有顯著的進步。

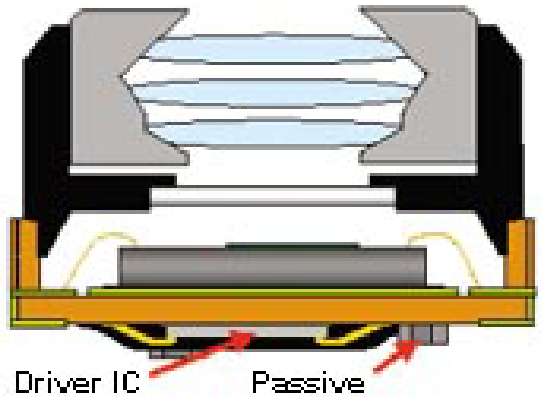
CIS:CMOS Image Sensor

SD & MMC SiP Package Solution



Camera Module - Stacked Chip Type

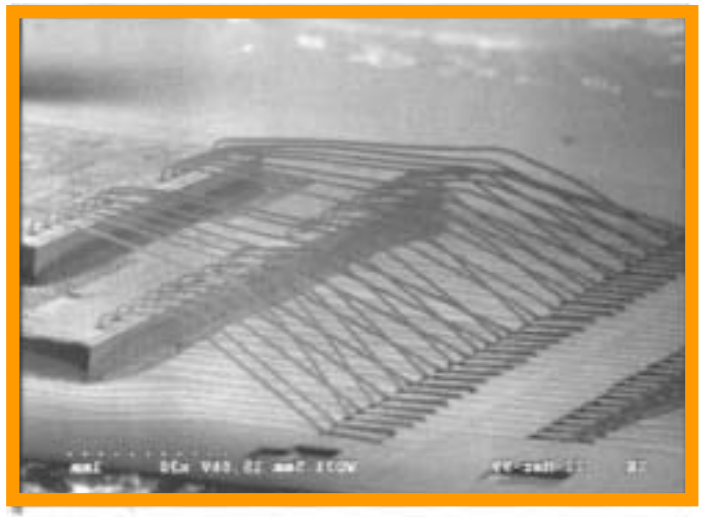


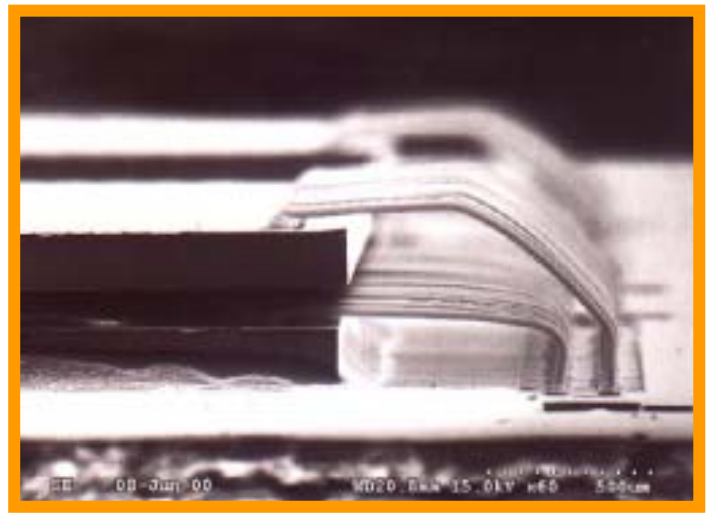


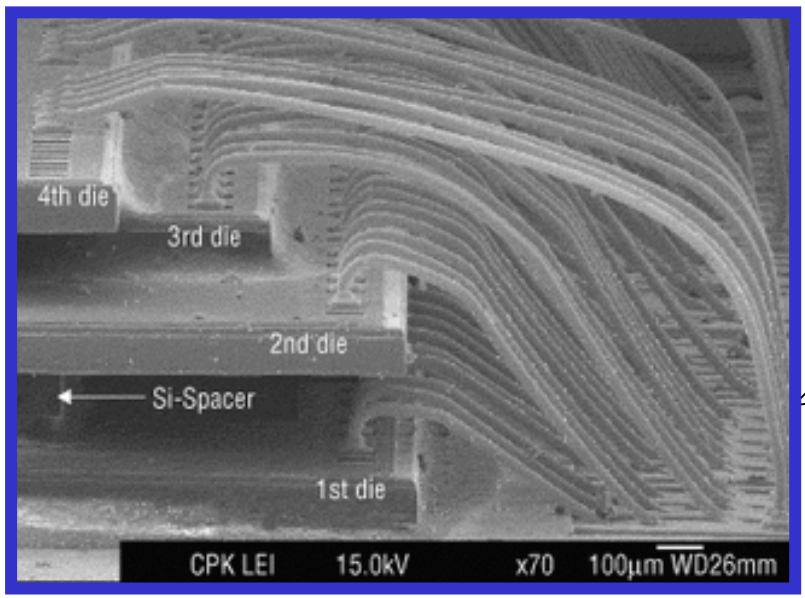
Fully integrated
CMOS image sensor

Source: Amkor

Stacked Chip /Die Solution





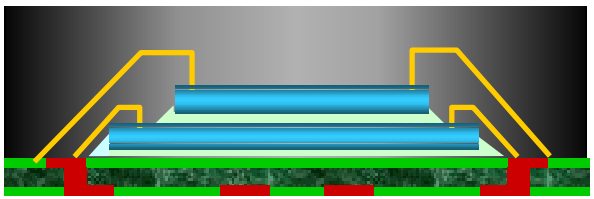


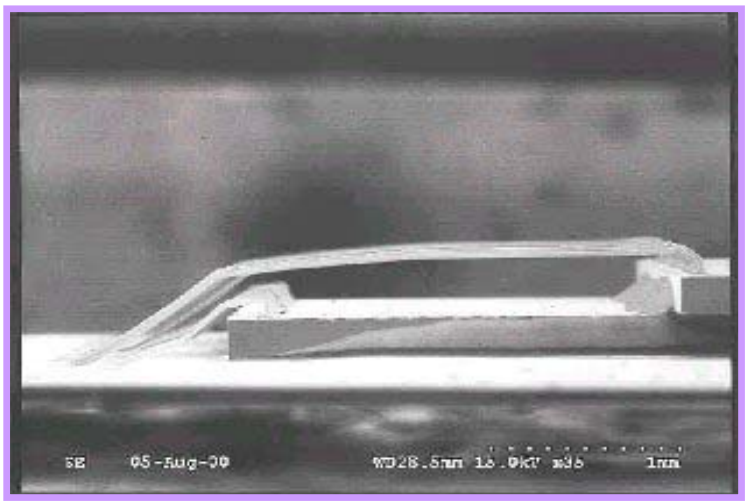
Inside this 1.4mm-thick CSP there are four 0.100mm-thick wire-bonded stacked-die. (Source: ChipPAC Inc.)

2 Dice Stacked Solution ~ Stacked Type

Structure :

Flash + SRAM
ASIC + Memory





Features & Profile :

- Die Attach Capability
- Wire bonding technology
- Die pad design and different looping group control
- Package Thickness: 0.9 mm Max (Estimation)
- Process Flow:

1st D/A -> 2nd D/A -> W/B -> M/D -> Forming

Application:

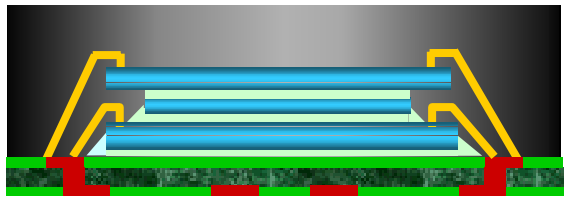
Telecommunication - cellular phone & wireless LAN

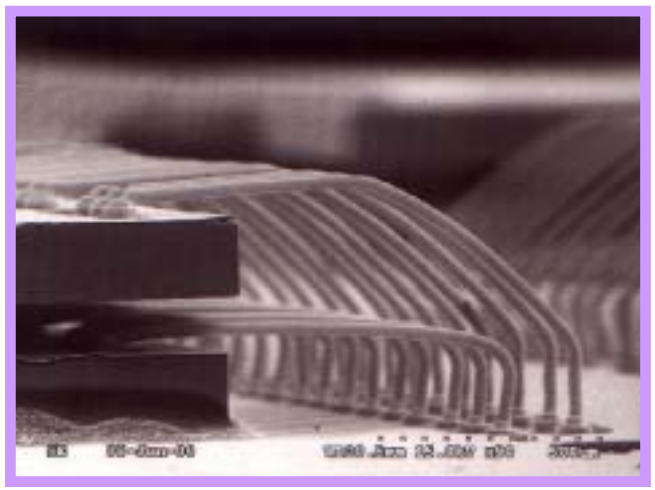
- FLASH + SRAM(16/2,32/4,32/8 MB)
- ASIC/Logic/DSP+ Memory

2 Dice Stacked Solution - Sandwich Type

Structure :

Double Density Package





Features & Profile :

- **Die Attach Capability**
- **Two or more identical dice stacked solution, wire bonding technology**
- **Critical wire looping control**
- **Package Thickness: 1.2 mm Max (Estimation)**
- **Process Flow:**

1st D/A -> Spacer Attach -> 1st W/B -> 2nd D/A -> 2nd W/B -> M/D -> Forming

Application:

- **Memory product - Compact Flash, PCMCIA Card**
- **Information Application - PDA, Digital Camera, MP3, IC Recorder**

Challenge on Stacked Chips -General

- KGD & package / module testing
- Wafer thickness specification (wafer thinning)
- Die bonder capability evaluation (upgrade to programming type)
- D/A material / method evaluation
- Spacer (sandwich type) design rule study
- W/B BGA looping study
- W/B SOB (stitch on ball) study (including cycle time and CPK evaluation)
- M/D material / method evaluation

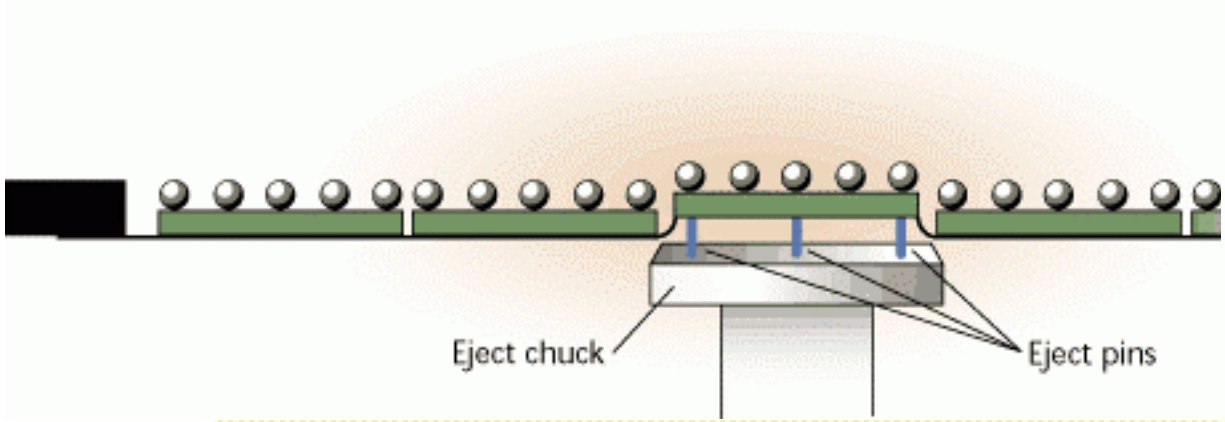
Challenge on Stacked Chips – Die Attach

- To stay within standard package heights, the stacked chips need to be thinned to the range of 50 - 125 µm.
- Gentle and controlled die pick-up procedure is needed
- High die placement accuracy is essential to mount the upper chip accurately onto the lower one. Inaccurate die placement can lead to electrical failure (wire shorts) and impacts the epoxy bleed out
- position and volume of the dispensed epoxy needs to be consistent. Excessive epoxy may cover the wire bonding pads, preventing a proper interconnection.

Using backside-coated wafers eliminates this problem since the adhesive is evenly spread on the backside of the top die and no epoxy/die offset can occur.

Solutions to Overcome Challenges

Some Concern for Picking up thin Chips



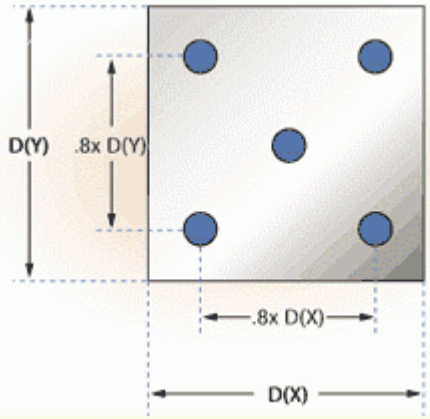
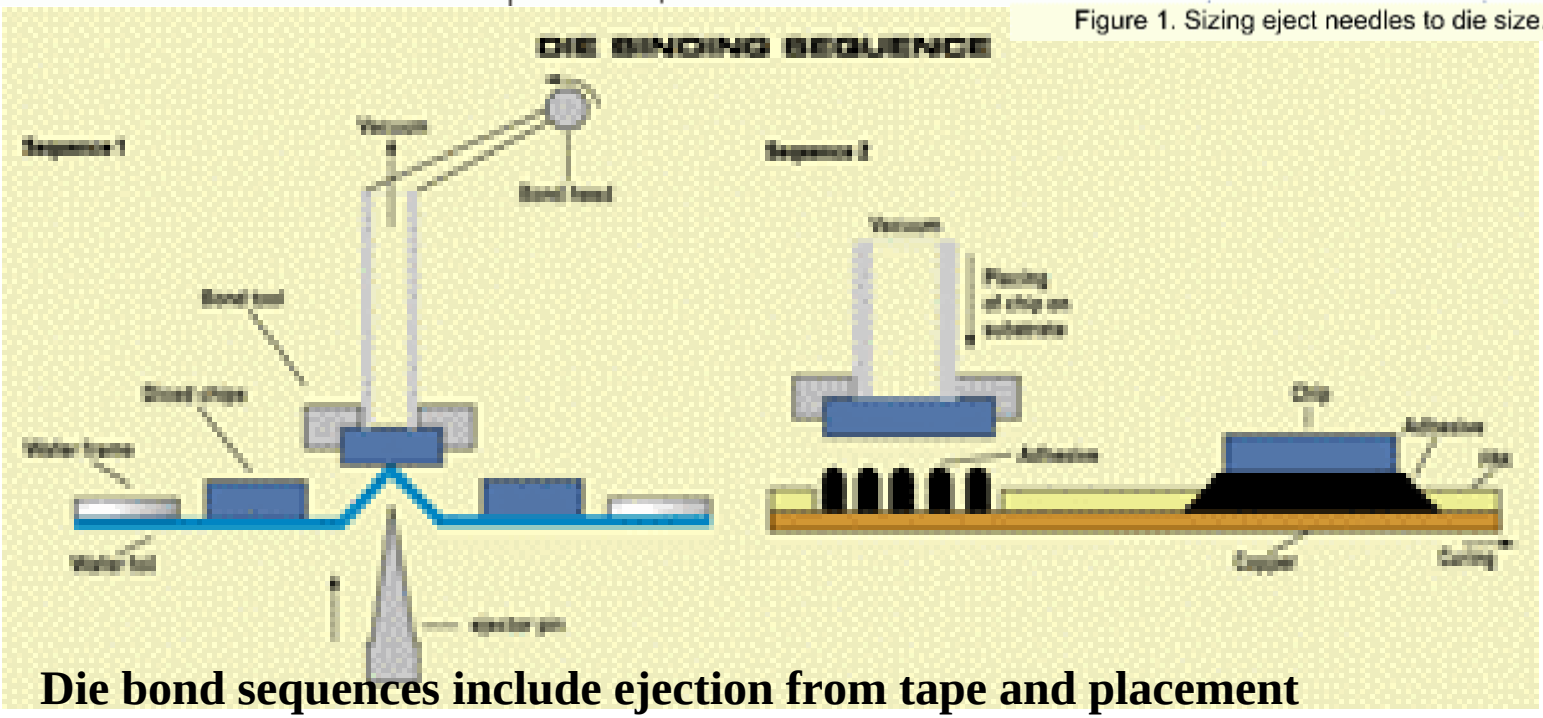


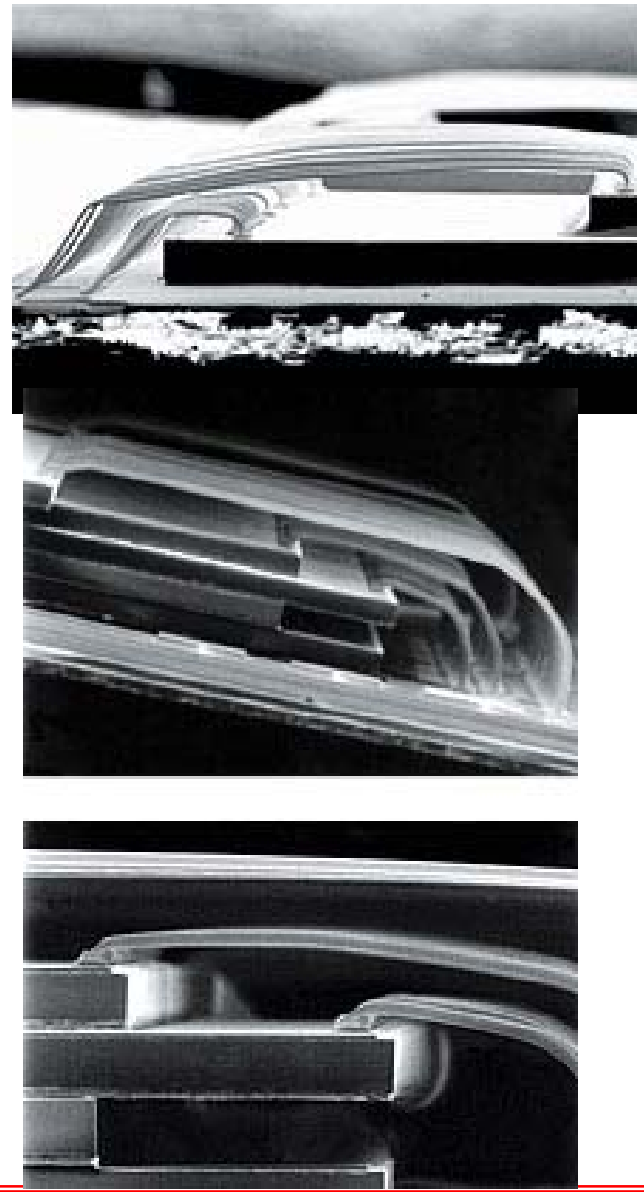
Figure 1. Sizing eject needles to die size.



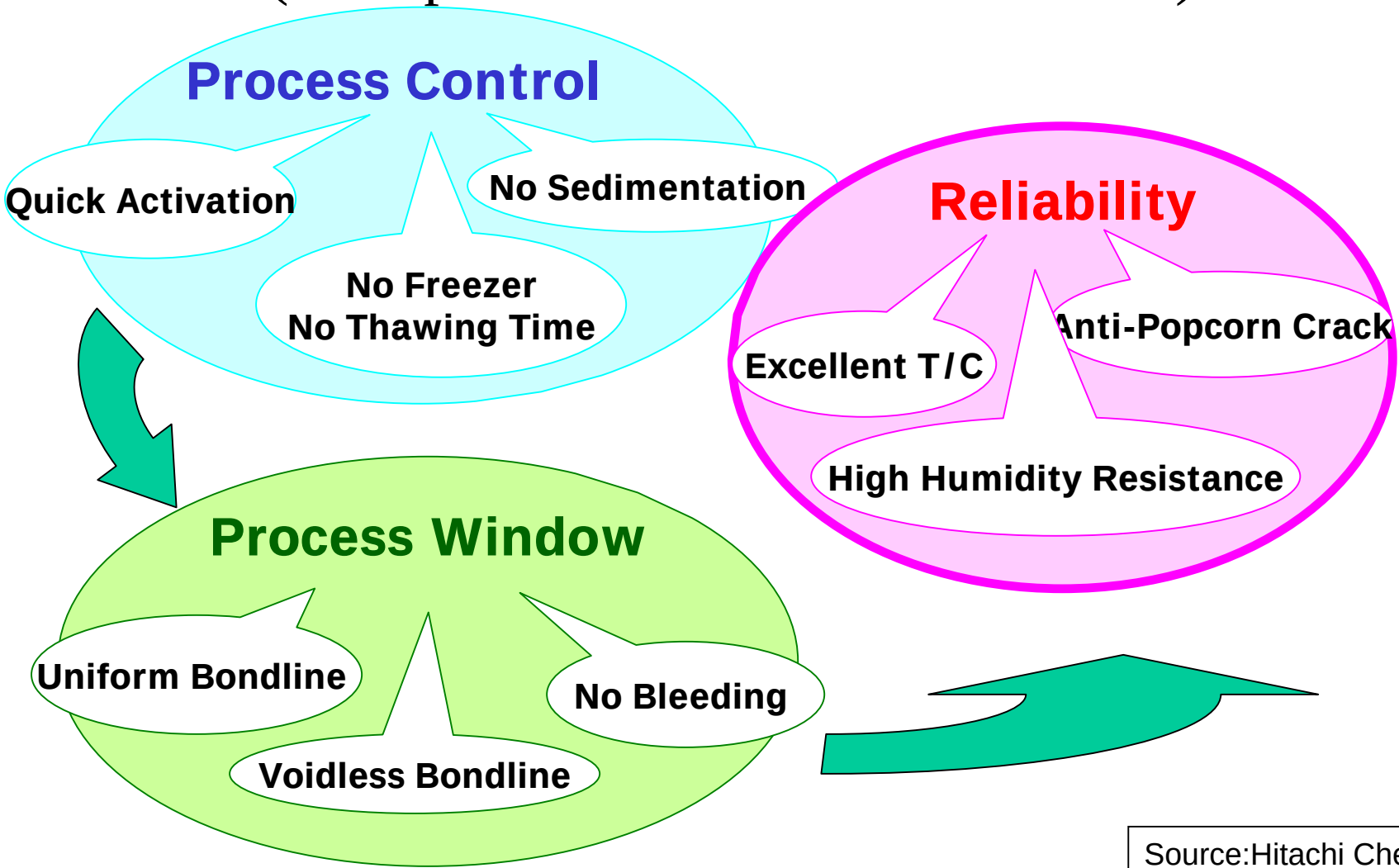
Die bond sequences include ejection from tape and placement

Stacked Chip Wire Bonding

- low loop and multi-level wire bonding loop clearance requirements, bonding to overhang unsupported die edges and loop resistance to wire sweep during molding
- A reverse ball bonder can achieve lower loops by placing a ball bump on the die, then bonding the wire from the substrate to the die. (Ball Stitch on Ball)



Advantage of Die Attach Film!!
(Comparison with Die Attach Paste)



Source:Hitachi Chemical

Process Advantages!

Paste

Storage −18℃

Thawing

Stirring

Dispense Control

Start

Film

Storage Room Temp.

~~Thawing~~

~~Stirring~~

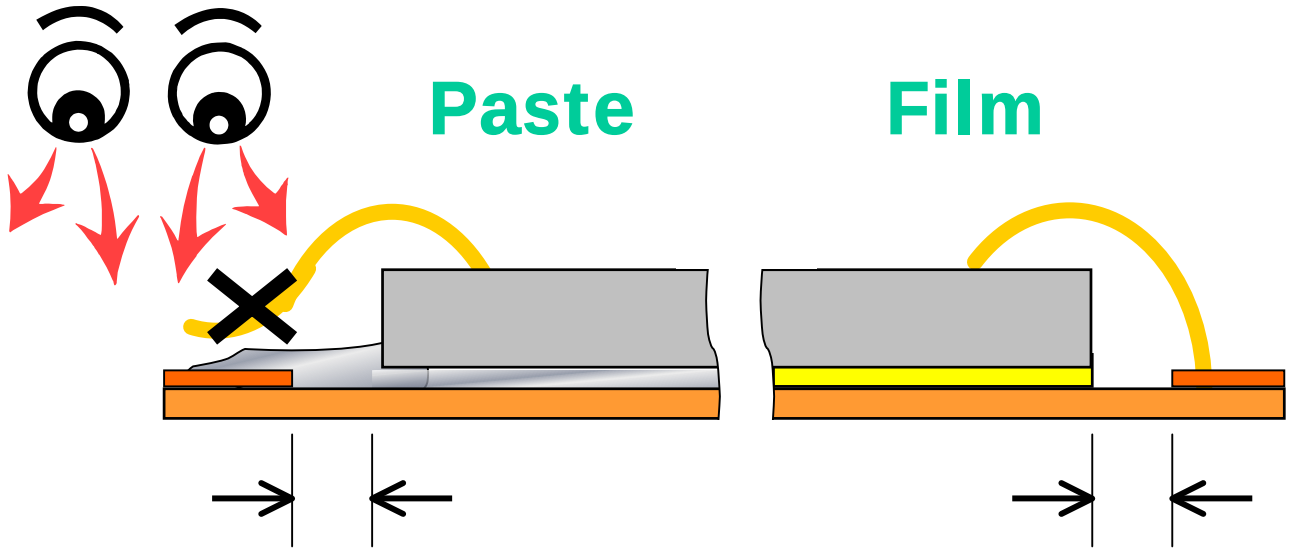
~~Dispense Control~~

Start

Source:Hitachi Chemical

Source:Hitachi Chemical

No Bleeds



KGD (Known Good Die)

放置來自不止一家矽供應商的晶片至單一構裝引出一些有趣的商業挑戰。一個OEM設計需要多家矽供應商提供晶片以整合MCP，所以在這些矽供應商之中必須存有商業關係，才能容許他們的晶片能與供應商的晶片構裝在一起。但這些商業關係仍難以建立，且必須對付及管理責任性與機密的議題。當一些矽供應商為一MCP/SiP提供晶片，誰該為全部MCP/SiP零件品質負責？就有缺陷的元件而論，誰該為問題解決來負責？在單一MCP/SiP中有著多樣矽供應者的晶粒，因為供應者擔負集成產品的最終責任，在有關於機密測試向量的可利用性需求上，時常在他們開始之前中止協商。許多矽供應商認為最終測試向量乃是他們的私有財產，不論什麼理由都不能釋放出去。

KGD (Known Good Die)

- What is KGD? According to the Die Products Consortium (DPC)*, "KGD is a process that provides the same levels of certainty . . . that the die product meets the equivalent quality and reliability targets as packaged parts."
- The process to make a KGD for a toy can be quite different from the process employed to make a KGD for an airplane guidance system.
- A die-form semiconductor product that meets or exceeds the product specifications, quality, and reliability required by the application
- Standard: EIA/JEDEC JESD49:Procurement standard for Known Good Die(KGD) This standard was created to facilitate the procurement and use of high-reliability semiconductor microcircuits or discrete devices provided in bare die form. It provides requirements and guidance to bare die suppliers for as-delivered performance, quality and long-term reliability expected of this product type.

Why is the topic of KGD important?

- Because there is a strong market for semiconductor products in stacked CSPs, SiP, MCM, DCA.
- There are more than one chip put in one package, the yield of each chip will give much influence on the package.

測試及預燒(Burn-In)議題

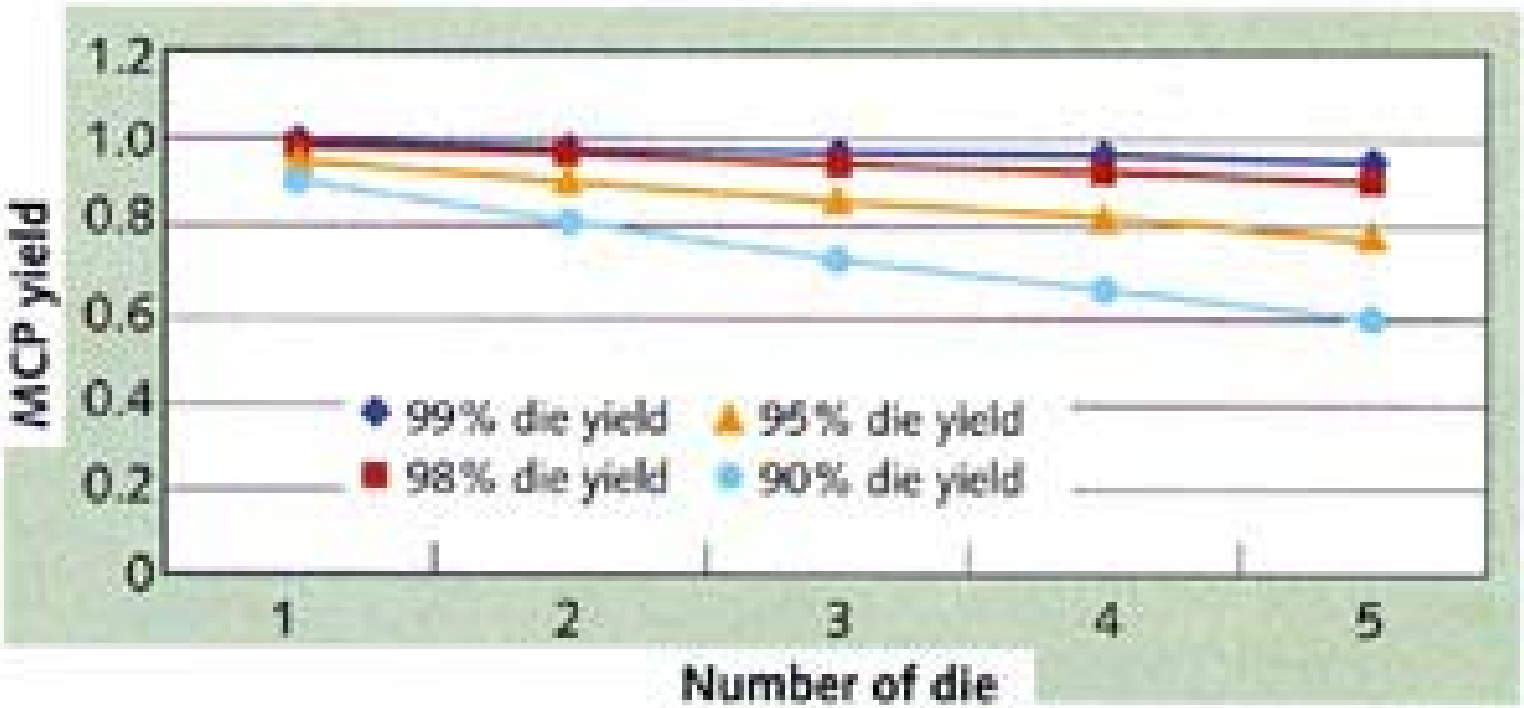
- 現今常見的單晶片構裝，在構裝層級的全部測試及預燒(Burn-in)不但滿足責任歸屬的議題，而且提供矽供應者在測試方法、工藝及向量上的完全控制。智慧財產權的重要成分與記憶體和邏輯元件二者皆有關連，將多樣的晶片置入一個單一積集構裝中將產生一些問題，因為在構裝之前，裸晶的全部測試及預燒，持續造成重大的技術與成本障礙。
- 當前的MCP解決方案通常須要在最終構裝組裝後作全部測試與預燒。這表示在構裝內的晶片所有矽供應商必須提供他們的測試向量以確保最終產品的品質。例如在手持產品上需求持續成長的DRAM元件，在晶片構裝之後需要預燒的程序以確保元件品質。預燒在個別晶片或晶圓層級仍是又貴又困難的，尤其對高容量的記憶體元件。

良率議題

- MCP組裝者通常依靠矽供應者的已知良好晶粒(known good die，KGD)程式來確保最終品質與他們MCP零件的良率。KGD程式在現今是一個較為普遍，且必需承擔的成本；就像穩固的工程保証金，較昂貴的晶圓測試設備及在模組組裝層級複合的良率損失要有較長的測試次數。此外，KGD程式不適用於尖端的IC加工或晶片設計。
- 雖然整合KGD與其他測試方法，使得現今的解決方案變得可行；但是在構裝前完整的晶粒測試仍是困難的。由於隨著在單一構裝內放置的晶片數目變化，使得成長良率也跟著惡化，晶粒良率對MCP的衝擊將可能導致成本的增加。
- 除了晶粒良率之外，在晶粒裝卸及構裝期間發生一些不可避免的附帶結果有可能導致極為昂貴的良率損失；因為受損的晶粒被包封了，所以一些好的晶粒最後都變成廢料。複合的良率損失隨著單一構裝中的晶粒數目增加而迅速增加，當晶粒或構裝的完整性無法完全的擔保時，馬上轉變為較高的產品成本。

良率 vs 晶粒數目

- 圖顯示就晶粒品質 / 良率中的變化而論，MCP良率如何隨著晶粒數目增加而迅速的降低。由於他們不僅依靠KGD技術，也依靠高度敏感的程序與組裝技術，當前的MCP解決方案並沒有解決這些議題。現今常見的MCP也排除了任何重工的可能性，進一步限制他們在低晶片數目及低價MCP的應用。一較低成本晶片在組裝成晶片堆疊之後被發現受損或缺陷，由於必須冒著丟棄高價晶片的風險，所以將任一高價晶片置入這些構裝中的障礙仍是很高。

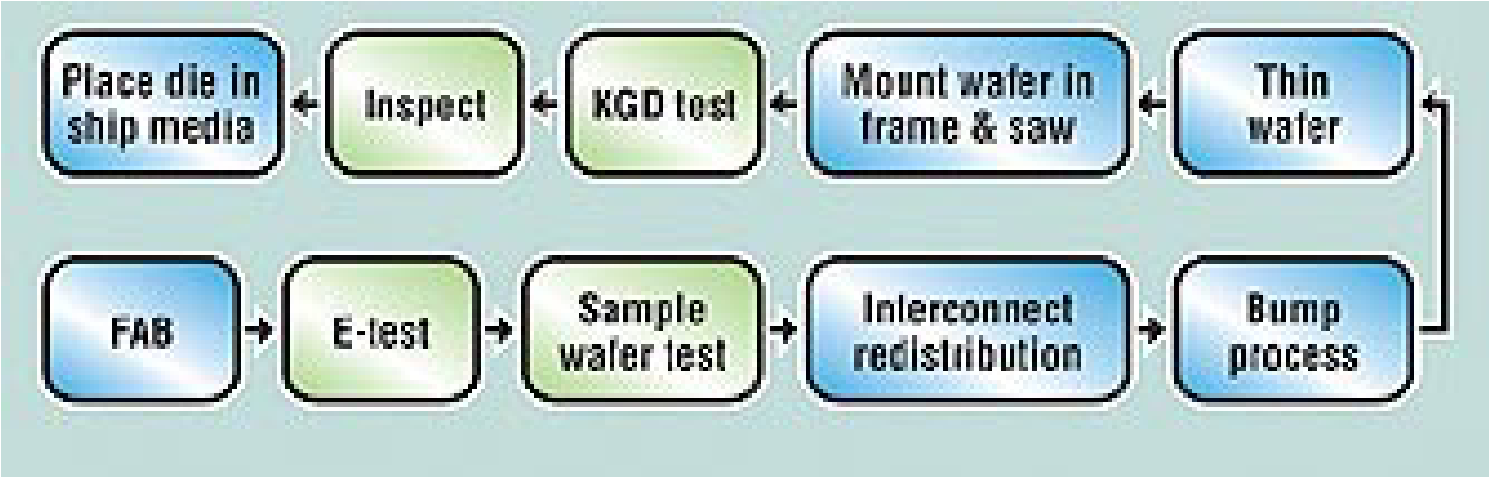


山不轉 路轉

- 必須克服將許多晶粒放置入一個構裝的技術障礙，而且必須解決根本的商業、策略及系統成本問題。MCP/SiP技術發展常常等待應用，不是因為技術的限制，而是由於晶片獲得之商業及策略的阻礙。這適用於全部的供應鏈，包括OEM、合約電子製造商及半導體製造商。MCP/SiP必須經由增加實用性來超越當前將許多晶片裝在一個小位置與形體中的成就。新興的解決方案也必須提供測試的靈活性、採購的多元性及組裝的適應性。
- 現今的MCP/SiP品通常將整合的構裝中，晶粒置於彼此表面，已知為晶粒堆疊(die stacking)。這樣通常是提供最低構裝成本的解決方案，其可以創造商業、策略及系統成本問題，如之前形容的**晶粒數目及複雜度增加**。
- **新興的解決方案藉由使用一種概念來克服許多這類障礙，此概念稱作構裝堆疊**(package stacking)，它提供一種能力，在最終的MCP構裝組裝之前，即能完成每一獨立晶粒或所選定晶粒群體的構裝級測試及預燒。一些解決方案的附加優點為，允許從多樣的供應商獲得個別的構裝晶粒，容許這類構裝結合在板級組裝上。
- 一個電子製造商也許從個別的邏輯裝置取得標準記憶體，以符合各種OEM記憶體組態的需求。舉個例子來說，**摺疊式構裝堆疊之解決方案**允許邏輯裝置及記憶體**可個別地獲得、測試及預燒**。其他新興技術也提供類似的特色，可能變得更好的解決方案，經由產生實際的、有成本效益的及迅速上市時機的低風險MCP/SiP。

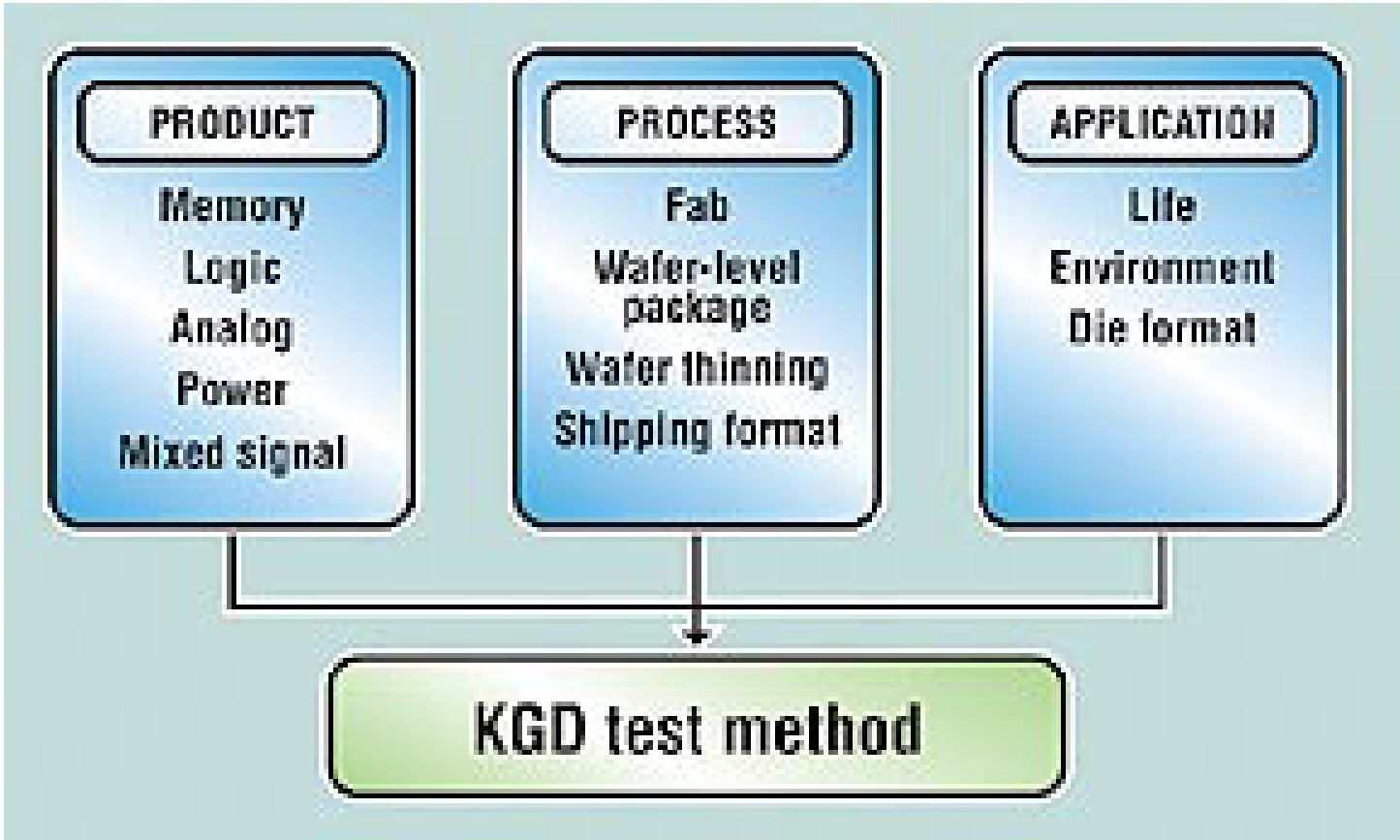
KGD Test & Burn In

KGD manufacturing flow



- Wafer fab and E-test are included in the flow because they can play a significant role in achieving working KGD.
- if the wafer is thinned slightly (or not at all), mounting for the saw may be done after KGD testing.
- S-CSPs need thin die to allow 2-3 to fit into a package form-factor of 1.4 mm high. This means that KGD for S-CSPs will have to be tested in a sawn wafer form in a frame after thinning.

What factors affect KGD testing



- Is there a single test method for KGD? not

Reliability

- **If the product or application requires burn-in to improve the reliability of the KGD.**
- **2 basic techniques for supplying it:**

  1. Burn in the die while they are still together on the wafer;

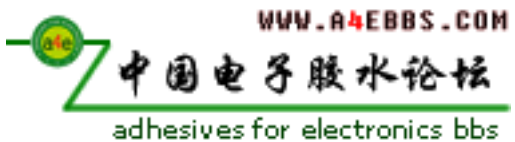
  2. Burn in the singulated die.
- **Wafer Burn-In : 2 similar techniques for wafer burn-in, employs sacrificial interconnect layers on the wafer to supply power and signal to the die. A second technique uses an interconnect layer on a film, with the wafer and film aligned and placed in the fixture.**
- **Another approach to improving reliability :remove die at KGD test that have a higher probability of failing during use.**

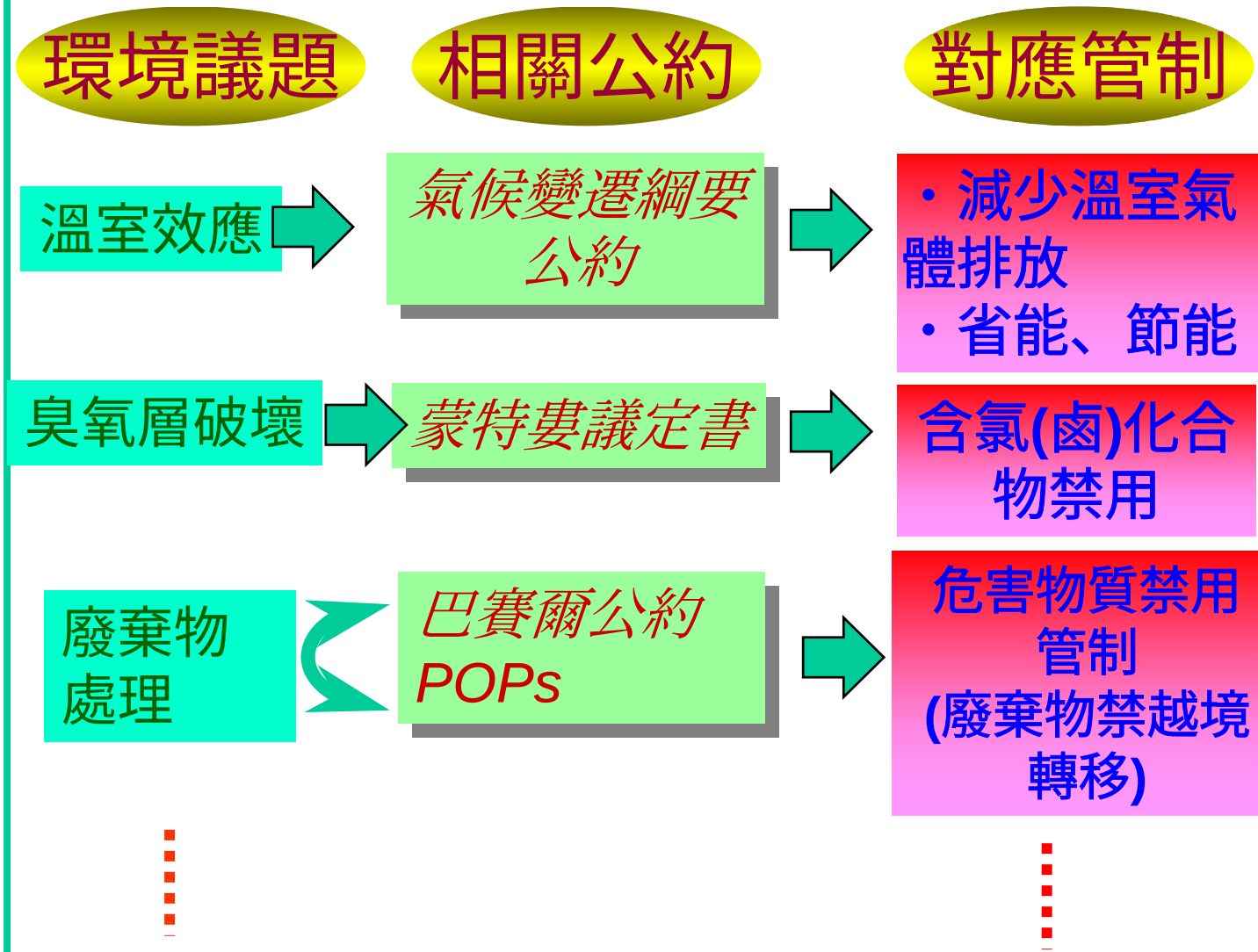
What are bare die burn-in and test alternatives?

- Three methods have emerged recently that manufacturers use to produce die products with high reliability at low cost:

1. Bare die temporary package.
2. Wafer probing with reliability screens.
3. Wafer-level burn-in and test (WLBT).

Lead Free & Green Package





電子材料對於環境造成的衝擊

- 氟氯碳化合物 (Chlorofluorocarbons , CFC)的使用, 會造成溫室效應 .
- 銲錫成份含鉛 ,會引起重金屬污染 .
- 光阻劑 (Photoresist) 中的溶劑,會造成化學溶劑污染 .
- 鹵素型難燃劑燃燒 , 會釋放出致癌的毒性氣體 .

綠色電子世界-無鉛製程

◆無鉛製程（Lead-Free）

現今無鉛銲錫的種類及應用

Solder	Melting point(℃)	Industry served	Company
SnAg	221-226	Automotive	Visteon(Ford)
SnAgBi	206-213	Military/Aerospace Consumer	Panasonic Hitachi
SnAgBiCu	Not available	Consumer	Panasonic
SnAgBiCuGe		Military/Aerospace	Sony
SnAgBiX	206-213	Consumer	Panasonic
SnAgCu	217	Automotive Telecommunications	Panasonic Nokia / Nortel / Toshiba/ Panasonic
SnBi	138	Consumer	Panasonic
SnCu	227	Consumer Telecommunications	Panasonic Nortel
SnZn	198.5	Consumer	NEC / Panasonic / Toshiba

無鉛銲錫 (Lead-Free Solder)

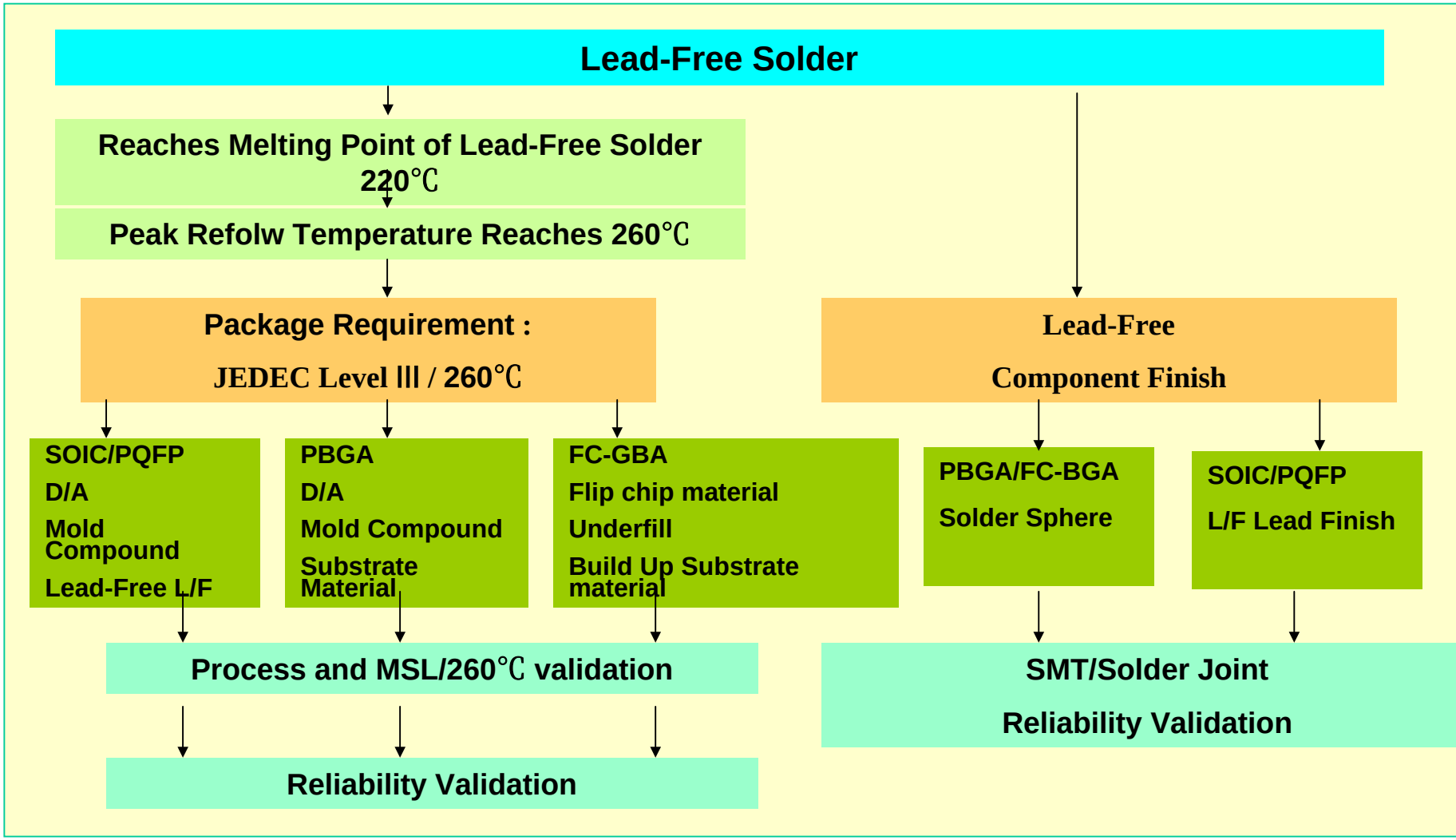
無鉛銲錫開發所需考慮課題

1. 無鉛銲錫熔點，高於傳統錫鉛銲錫 ．將會對電路基板材料及其附屬元件構成重大的影響 ．
2. 如果僅單獨改變使用無鉛銲錫合金 ，將會降低基板的可靠度.
3. 然而對於銲錫溫度較高之問題 ，基板材料必須注意 ．

   (a) Z軸膨脹 (Z-axis Expansion) - - 影響通孔可靠度 (Through Hole Reliability) .

   (b)裂解(Decomposition)問題 ．
4. 從提煉過程分析 ，無鉛銲錫材料中添加的Ag ，Bi ，Sb等元素都與Pb同時存在 ，亦即無鉛銲錫之使用 ，並不會減少鉛礦開採對環境衝擊

無鉛銲料對半導體封裝之衝擊



無鹵素材料(Halogen-Free Material)

定義：是指整體材料所包含之氯含量< 900ppm和溴含量< 900ppm,才能 作為環保型材料開發 .

無鹵材料開發過程中，主要根據四個概念進行開發

(1)難燃性需符合UL94-V0標準

(2)不含有鹵素

(3)不含有銻元素

(4)不含有紅磷

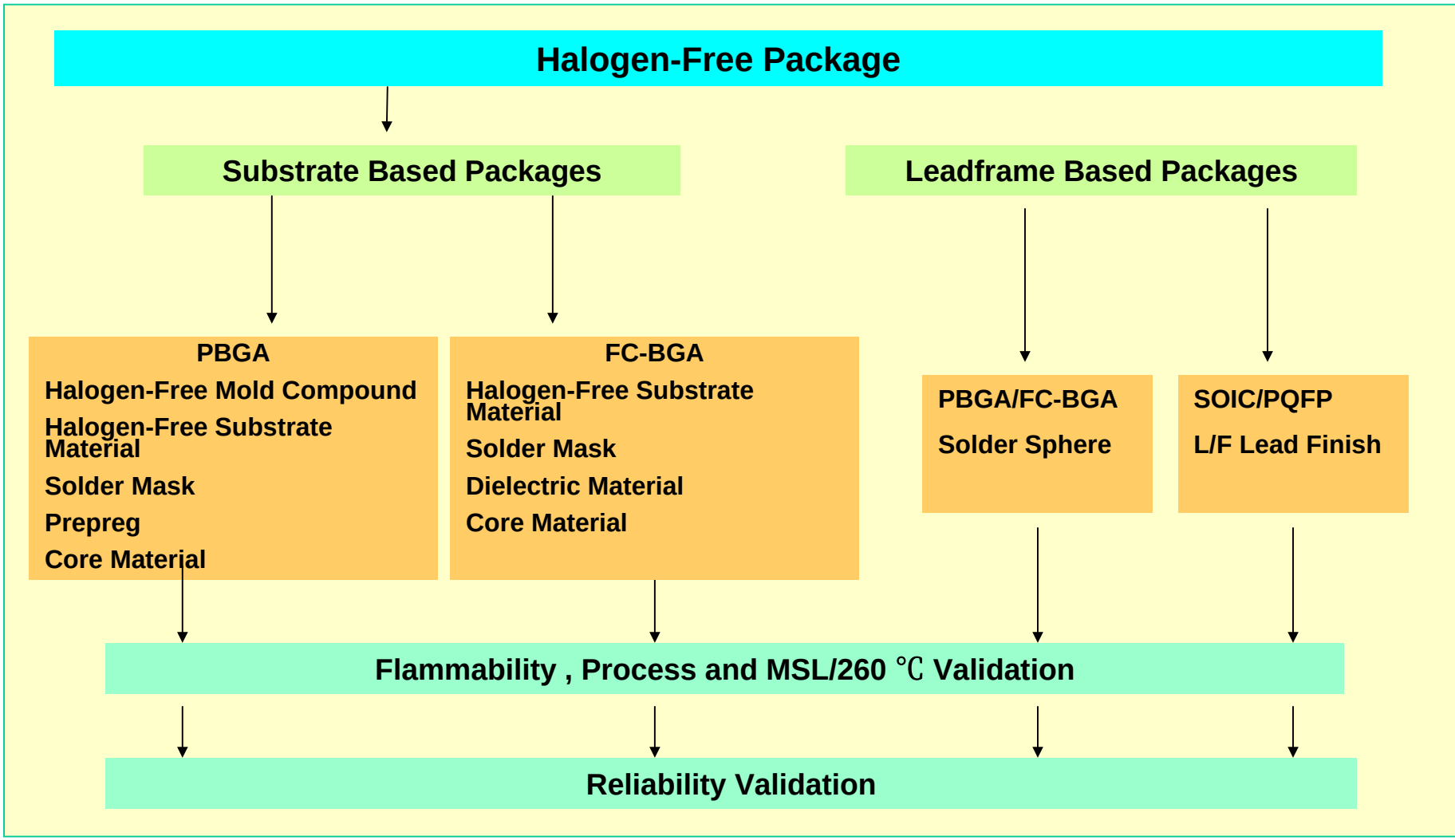
綠色電子世界-無鹵素構裝

◆無鹵素構裝（Halogen-Free）

無鹵素模壓樹脂之難燃劑比較表

Type	Main Material	Advantage	Disadvantage
Phosphorous type	1.poly ammonium phosphate 2.Phosphoric ester 3.Triazine derivative 4.Red phosphorous	Good flame Retardation	1.High water absorption and low water proof 2.Electric properties drop 3.Much PO^{4-} ion
Nitrogen type	1.Melamine 2.Cyanuric acid triagine derivative	Decreasing smoke	1.Poor flame retardation 2.Plastic properties drop (SF, strength,etc)
Metal hydrate type	1.Aluminium hydroxide 2.Magnesium hydroxide 3.Borate	1.High Safety 2.Decreasing smoke	1.Poor flame retardation 2.Plastic properties drop (SF, strength,etc)
Metal oxide type	1.Molybdenum 2.Tungsten oxide		1.Poor flame retardation 2.Plastic properties drop (SF, strength,etc)

無鹵素材料對半導體封裝之衝擊



環保材料開發過程的認知與瓶頸

1. 此環保材料對於人類及環境是否較不具毒性或危害性?
2. 目前開發出來的無鉛銲錫具有較高的熔點 ， 基板材料被迫必須往高Tg發展 ， 而其中組裝的元件是否能承受住較高的加工溫度 ， 也是一大問題.
3. 大部份無鉛銲錫的產品皆為三至四種金屬元素所組成的合金 ， 是否有 一定的再現性 .

Two consortiums aim for the Advanced Package

- APiA (Advance Package and interconnect Alliance)
- APiA, the newest consortium, is focused on "accelerating the development and implementation of commercially viable, comprehensive and risk-free packaging solutions that address the escalating manufacturing and performance challenges of leading-edge chipmakers worldwide. As such, the alliance will concentrate on enhancing the productivity of the equipment and process solutions critical for advanced packaging and interconnect processes, as well as developing guidelines and standards to enable easy adoption of these sophisticated solutions."

Two consortiums aim for the Advanced Package-cont.

- **SECAP** (Semiconductor Equipments Consortium Advanced Package)
- SECAP's mission is "to support the advanced packaging industry by delivering optimized process equipment for wafer bumping, wafer level packaging and HDI technology. The membership of SECAP is limited to equipment and material suppliers in order to maintain SECAP as an efficient and trustworthy resource to the advanced packaging industry."

ITRS 2003 Assembly & Packaging Challenges

For Your Reference !!
Please read at your convenience !!

ITRS 2003 Assembly & Packaging Challenges (1)

Near term : till 2010

Difficult Challenges ≥ 45 nm/Through 2010	*Summary of Issues*
Improved Organic Substrates	Tg compatible with Pb free solder processing Increased wireability at low cost Improved impedance control and lower dielectric loss to support higher frequency applications Improved planarity and low warpage at higher process temperatures Low-moisture absorption Low-cost embedded passives Substrate cost is barrier to flip chip wide spread adoption today Increased via density in substrate core Alternative plating finish to improve reliability
Improved Underfills for Flip Chip on Organic Substrates	Thermal performance and thermal coupling between parts Materials which enable integration of SMT, varying semiconductors, and substrate types reliably Thin die, stack die, very large and very small die, passives component integration, SAW, shielding interconnect process Narrowing gaps Higher bump densities

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ITRS 2003 Assembly & Packaging Challenges (2)

Near term : till 2010

Coordinated Design Tools and Simulators to address Chip, Package, and Substrate Co-design	Mix signal co-design and simulation environment Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis Electrical (power disturbs, EMI, signal integrity associated with higher frequency/current and lower voltage switching) Commercial EDA supplier support System level co-design is needed now. EDA support for "native" area array is required to meet the Roadmap projections. Educational programs required to train engineers in these technologies/requirements.
Impact of Cu/low κ on Packaging	Direct wirebond and bump to Cu Bump and underfill technology to assure low-κ dielectric integrity Improved mechanical strength of dielectrics Interfacial adhesion Reliability of first level interconnect with low κ Mechanisms to measure the critical properties need to be developed. Probing over copper/low κ due to damage and bonding over probe mark
High Current Density Packages	Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling. Whisker growth Thermal dissipation

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ITRS 2003 Assembly & Packaging Challenges (3)

Long term : beyond 2010

Difficult Challenges <45 nm/Beyond 2010	*Summary of Issues*
Package Cost does not follow the Die Cost Reduction Curve	Margin in packaging inadequate to support investment required to reduce cost
Small Die with High Pad Count, High Power Density, and/or High Frequency	Current density, operating temperature, etc for these devices exceed the capabilities of current assembly and packaging technology
High Frequency Die	Substrate wiring density to support >20 lines/mm Lower loss dielectrics—skin effect above 10 GHz "Hot spot" thermal management needs to be addressed before 2007. There is a "brick wall" at five-micron lines and spaces. Design TWG would like to have an upper bound on thermal management capability of future packages.
Close Gaps between Substrate Technology and the Chip	Interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology Production techniques will require silicon-like production and process technologies after 2005.

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ITRS 2003 Assembly & Packaging Challenges (4)

Long term : beyond 2010

System-level Design Capability to Integrated Chips, Passives, and Substrates	Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. Complex standards for information types and management of information quality along with a structure for moving this information will be required. Hardware only This is also an issue before 2007.Embedded passives may be integrated into the "bumps" as well as the substrates.
New Device Types (Organic, Nanostructures, Biological) that require New Packaging Technologies	Organic device packaging requirements not yet define (will chips grow their own packages) Biological interfaces will require new interface types
Bumpless area array technologies will be needed during this period. Face to face packages and other 3D packages are examples. High frequency, low power and low profile are driving forces	

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Questions & Answer ?

Any Question is welcome !